Statements of Support for the UCIe 3.0 Specification

Analog Devices

“The enhancements introduced in UCIe 3.0 will enable RF Data Converters to integrate into the UCIe ecosystem. At Analog Devices, we view UCIe as a foundational element of our Chiplet Platform strategy, particularly for high-performance applications in Aerospace & Defense, Instrumentation and Communications.

The addition of features such as Vendor-defined signals and Variable Rate support broadens UCIe’s applicability to real-time streaming, making it well-suited for RF data converters. In collaboration with industry partners through JEDEC, we are also committed to leveraging these features in the JESD204E standard to ensure robust converter data transmission over UCIe.”

- *Henil Langalia, Staff Engineer, Analog Devices and JESD204E Task Group Chair*

Arm

“Chiplets are critical to scale system performance and efficiency, especially as AI workloads demand more bandwidth, modularity, and design reuse. UCIe 3.0 introduces important capabilities, including higher link speeds and richer manageability, that help support protocols like AMBA CHI C2C for coherent, multi-chip configurations. These enhancements mark a constructive step toward broader interoperability and practical chiplet deployment across markets.”

- *Dong Wei, Standards Architect and Fellow, Arm*

Astera Labs

“The UCIe 3.0 specification's 64 GT/s performance arrives at the perfect moment as AI infrastructure explodes beyond traditional server boundaries into the rack-scale era. The specification's enhanced bandwidth density and improved power efficiency provide a crucial foundation for the disaggregated, modular architectures that define the future of AI computing at rack scale.”

- *Casey Morrison, Chief Product Officer, Astera Labs*

Ayar Labs

“The UCIe 3.0 specification represents another important milestone for the interconnect chiplet ecosystem. By increasing maximum bandwidth rates to 48 and 64 GT/s per channel, UCIe 3.0 enables higher shoreline bandwidth density for scale-up connectivity. These increasing data rates are critical to addressing the growing interconnect bandwidth demands of GPUs and ASICs in AI applications. At Ayar Labs, our TeraPHY™ optical I/O chiplet roadmap is aligned with the UCIe specification to drive broad adoption and manufacturability of co-packaged optics in next-generation AI architectures.”

– *Vladimir Stojanovic, Co-Founder and CTO, Ayar Labs*

Cadence

“Cadence is proud to continue our close collaboration with the UCIe Consortium in advancing open chiplet standards. The UCIe 3.0 specification’s leap to 64 GT/s, along with its enhanced manageability and system-level flexibility, reflects the industry’s growing need for scalable and interoperable High Performance Computing solutions. As a provider of widely published and silicon-proven UCIe IPs, we’re excited to support the next wave of high-performance chiplet innovation—accelerating progress from silicon to systems.

- *Ravi Venigalla, Vice President of R&D, Cadence*

Google

"Google applauds the release of the UCIe 3.0 specification, which is critical for next-generation AI and HPC infrastructure. The leap to 64 GT/s provides the bandwidth necessary to scale demanding workloads. Enhanced manageability features like fast throttle and early firmware download ensure the reliability and efficiency of complex, multi-chip systems. We remain committed to open standards like UCIe that foster a flexible, interoperable, and innovative chiplet ecosystem."

- *Jérôme Glisse, Software Lead and UCIe Manageability & Security Workgroup Co-chair, Google*

Intel

"UCIe 3.0 advances chiplet interconnect with higher bandwidth, lower latency, and enhanced system manageability—meeting the escalating performance demands of modern heterogeneous compute. Intel's leadership in open standards continues to drive scalable, efficient architectures across AI, data center, and edge applications."

- *Dimitrios Ziakas, VP & GM, Data Center Platform Architecture, Intel Corporation*

Microchip

"UCIe 3.0 extends UCIe 2.0 capabilities for manageability, debug and test as well as enabling 3D package support allowing for increased bandwidth density and power and efficiency allowing improved performance and management desired for chiplet technology advancement. The features in this latest version of the open standard shows continued industry investment and evolution for die-to-die interconnect."

- Brian McCarson, Corporate Vice President of Data Center Solutions Business Unit, Microchip

Neuron IP

"We're proud to support the UCIe Consortium and the release of the UCIe 3.0 Specification. At Neuron IP, we've seen firsthand how a unified, open standard like UCIe can unlock new possibilities in advanced packaging, heterogenous technologies, and chiplet-based architectures. As we continue to develop UCIe IP across multiple technology nodes, this next evolution of the spec aligns perfectly with our goal: to help our customers build faster, more efficient, and sustainable multi-die systems. By standardizing higher data rates and introducing expanded optional features, UCIe 3.0 represents a big step forward - for us, for the ecosystem, and for the future of semiconductor integration."

- *Saman Sadr, President & CEO, Neuron IP*

NVIDIA

“The UCIe 3.0 specification marks a significant leap forward for the world’s most interoperable chiplet interconnect standard. With new link speeds of 48 GT/s and 64 GT/s, UCIe 3.0 enables the highest performance chiplets, allowing different compute elements to communicate with extreme efficiency. NVIDIA is committed to UCIe as the open chiplet standard and continues to support its evolution to meet the demands of next-generation heterogeneous computing."

- Ashish Karandikar, Vice President of Engineering, NVIDIA

Rebellions

“Rebellions proudly announces its comprehensive support for the UCIe 3.0 Specification. Building on our AI inference ASICs powered by UCIe 2.0, the new standard unlocks faster data rates(48/64GT/s) and critical system features that further strengthen the performance and scalability of our chiplet-based NPU solutions. Key enhancements in UCIe 3.0—such as Early Firmware Download and Emergency Shutdown—bring faster initialization, greater system flexibility, and improved safety across deployment environments. These advances directly support the optimized deployment of Rebellions' NPU cards, servers, and rack-level systems for high-performance on-premises AI infrastructure. Rebellions remains deeply committed to fostering a vibrant chiplet ecosystem. Our continued innovation and strategic partnerships including crucial collaborations on next-gen HBM solutions with leading Korean enterprises ensure that we deliver future-ready AI hardware solutions—built on the robust foundation of UCIe 3.0.”

- *Jinwook Oh, CTO, Rebellions*

Samsung Electronics

“As designs grow more complex, chiplets are emerging as the leading architecture for next-gen HPC and AI – driving the growing importance of the UCIe standard. As a Promoter Member and Board participant, Samsung has supported UCIe from the start. With UCIe 3.0, we’re enabling customers to achieve greater bandwidth and density in larger, more efficient system-in-package designs – leveraging our expertise in silicon, memory, and advanced packaging to shape the future of chiplet interoperability.”

- Ben Hyo Gyuem Rhew, Vice President and Head of the IP Development Team, Samsung Electronics

Siemens EDA

“Building on the long-standing relationship our Avery Verification IP team has with the UCIe standards body, and our collaboration with the leading innovators in UCIe semiconductor design, Siemens EDA is once again a key contributor for the newest version of UCIe technology. We welcome this latest release of the UCIe solution from the UCIe Consortium, and we are seeing the impact this has already with our collaborations with leading edge users to build new, exciting applications across all markets for chiplet makers, integrators and foundry providers.”

- *Gordon Allan, Director of Questa One Avery Verification IP, Siemens EDA*

Synopsys

“The UCIe 3.0 specification, offering higher bandwidth and enhanced manageability features, is accelerating high-performance, die-to-die connectivity for demanding applications like AI. Synopsys' complete, high-quality, power-efficient UCIe IP solution, silicon-proven in customer designs with proven interoperability, supports the UCIe 3.0 standard at 64Gbps. The IP solution enables designers to confidently drive innovation for next-generation multi-die designs.”

- *Neeraj Paliwal, Senior Vice President of IP Product Management, Synopsys*

Texas Instruments

“As a leader in high-speed, high-performance data converter technology, Texas Instruments recognizes the critical importance of an industry-standard, high-speed and low-power chiplet interface to help engineers accelerate innovation and simplify system integration. UCIe™ enables our customers to integrate our high-speed analog conversion expertise into their systems more easily, dramatically reducing design complexity and time-to-market. We are proud to support UCIe™ by adding devices designed to UCIe™ specifications to our broad portfolio of data converters and are excited to help shape the next generation of chiplet-based systems that this standard will make possible.”

- *Matthew Hann, Product Line Manager, RF Sampling and High-Speed Data Converters, Texas Instruments*

Truechip

“At Truechip, we see UCIe as a foundational step in the evolution of chiplet-based architectures. The UCIe Consortium plays a critical role in driving industry alignment and standardization, enabling seamless interoperability and scalability across vendors. UCIe technology directly addresses the need for high-bandwidth, low-latency die-to-die connectivity, empowering innovation in AI, HPC, and data-centric applications. As a company committed to providing robust Verification IP solutions, Truechip supports the UCIe Specification to accelerate time-to-market and ensure compliance in next-generation designs. UCIe not only advances the semiconductor ecosystem but also aligns with our mission to make design verification faster, smarter, and more reliable.”

— Nitin Kishore, CEO, Truechip

TSMC

“TSMC is delighted with the introduction of the UCIe 3.0 specification, a significant milestone in advancing chiplet interconnect technologies. The release of UCIe 3.0 presents exciting opportunities for ecosystem-wide collaboration, enabling 3D IC designs to achieve new heights in performance and power efficiency. We congratulate the UCIe Consortium on this achievement and reaffirm our commitment to advancing AI innovation by enabling cutting-edge design solutions in collaboration with our Open Innovation Platform® (OIP) partners and customers.”

- *Lluis Paris, Senior Director of Ecosystem and Alliance Management, TSMC North America*

UniVista

“UCIe is an innovative die-to-die (D2D) interconnect technology that delivers interoperability between different designs and packaging technologies with its full-stack solution covering software, management, security, and testing. As a contributor of the UCIe Consortium and its working groups, UniVista is proud to integrate our UCIe IP subsystem into over 30 customer’s designs in the last three years. The Consortium has released UCIe 2.0 which shows short latency, high bandwidth density, power efficiency and enhanced stability, and enabled more companies to adopt UCIe as Die-to-Die interface in their design. The newly released UCIe 3.0 introduces more comprehensive enhancement and support 48GT/s and 64GT/s. UniVista will continue the IP development of new version UCIe and remains committed to supporting the advancement and widespread adoption of UCIe technology.”

- *Mao Liu, Vice President, UniVista*