UCIe Consortium Members – Statement of Support for UCIe® 4.0 Specification

AMD
“UCIe 4.0 marks an important evolution from chiplet connectivity to system-level integration. By advancing memory connectivity, power and bandwidth efficiency, and the manageability and security of chiplets working together, the specification provides a stronger foundation for increasingly sophisticated chiplet-based designs. For AMD, these capabilities can help us continue scaling chiplet innovation across our portfolio while optimizing systems for a growing range of workloads and performance requirements.”
Anwar Kashem, Corporate Vice President of I/O Architecture, AMD

Arm
"Integrating compute, memory and specialized accelerators efficiently is essential to building the next generation of heterogeneous systems. Arm is advancing open chiplet innovation through technologies like AMBA C2C, while industry standards such as UCIe help contribute to broader interoperability and give silicon designers greater flexibility to build differentiated solutions.”
Dong Wei, Fellow and Lead Standards Architect, Arm

Astera Labs
"Memory and power are two walls setting the limits of AI infrastructure today, and UCIe 4.0 pushes both back. A standardized on-package memory link reaches up to 93.75% data efficiency, and the power-optimized profile delivers up to 30% greater energy efficiency at 64 GT/s. With security built into the chiplets, silicon from any vendor can join the system, so every builder can assemble the AI infrastructure their way."
Casey Morrison, Chief Product Officer, Astera Labs

Cadence
“UCIe 4.0 provides critical building blocks for the next generation of Physical AI systems. “Standardized memory connectivity and co-optimized interfaces enhance right-sized inference operation, while chiplet identity, secure management, and lifecycle controls help establish trusted execution. With enhanced support for scalable 2D and 3D heterogeneous integration, reset coordination, and runtime monitoring, UCIe 4.0 also strengthens the spec-to-silicon path. Cadence is committed to helping customers realize these capabilities in interoperable, secure, and production-ready chiplet platforms.”
David Glasco, vice president of the Silicon Solutions Group, Cadence

Google
"Google applauds the UCIe Consortium on the release of the UCIe 4.0 specification. In large-scale AI systems, every watt spent moving data between chiplets is a watt not available for compute, which makes die-to-die interconnect power a first-order design constraint. The new UCIe Co-optimized Profile addresses this head-on, delivering high-bandwidth, short-reach, in-package connectivity at a fraction of the power of a general-purpose link. Google is proud to have helped drive this work and remains committed to UCIe as the open standard for an interoperable, multi-vendor chiplet ecosystem."
Kok-Hong Chan, Silicon Engineer, Google and UCIe Board member

Honda R&D Co., Ltd.
“Honda welcomes the release of the UCIe 4.0 specification, which enhances system-level reliability for automotive applications, as an important step toward a more open and interoperable chiplet ecosystem. As semiconductor architectures become increasingly complex, industry-wide standards are essential to enable scalable, efficient, and reliable system integration. UCIe 4.0 will help accelerate innovation by providing a common foundation for greater design flexibility and collaboration across the industry. Honda believes that these advancements will also contribute to the evolution of automotive semiconductor platforms, supporting the increasing performance, functionality, and reliability requirements of future mobility. Honda looks forward to continuing to contribute to the advancement of the UCIe ecosystem and technologies that support the future of mobility.”
Tomoya Nishino, General Manager, Honda R&D Co., Ltd.

Intel
“UCIe Consortium continues to advance chiplet integration by improving power efficiency and increasing bandwidth density. The UCIe 4.0 specification introduces a standardized, scalable, high-performance on-package memory interface between SoCs and memory logic chiplets, providing an efficient way to scale memory bandwidth. With new manageability and security capabilities, UCIe 4.0 also expands beyond chiplet connectivity to address broader system-level requirements. Intel is proud to be a contributing member of the UCIe Consortium and to help advance the standard for chiplet connectivity, benefiting both Intel and the broader chiplet ecosystem.”
Dr. Debendra Das Sharma, Intel Senior Distinguished Engineer, Chairman of the UCIe Consortium, Intel

Keysight Technologies
“As chiplet ecosystems expand, interoperability must move from specification to proven implementation. The UCIe Consortium provides the common framework needed to enable a scalable, multi-vendor chiplet ecosystem. As a UCIe member, Keysight bridges virtual design and physical validation, helping turn open standards into proven interoperability and accelerating multi-vendor chiplet innovation.”
Pedro Merlo, Manager of Strategic Planning, Network and Data Center Solutions, Keysight Technologies

MIRISE Technologies Corporation
"MIRISE Technologies welcomes the release of the UCIe 4.0 Specification as an important milestone toward an open and interoperable chiplet ecosystem. For future automotive systems, chiplet technology has the potential to enable flexible and scalable SoC architectures by integrating dies with different functions and technologies. At the same time, automotive applications require high levels of functional safety, reliability, and system manageability. We welcome the continued evolution of the UCIe specification, enabling UCIe technology to be applied more broadly to automotive applications. MIRISE Technologies will continue to contribute to the advancement of UCIe and interoperable chiplet technologies, accelerating their adoption in future automotive SoCs."
Satoru Taniguchi, Member of the Board, MIRISE Technologies Corporation

Neuron IP
“Neuron IP is proud to once again support the UCIe Consortium with the release of the UCIe 4.0 Specification. The growing industry adoption of UCIe, across an expanding ecosystem of semiconductor companies, technologies, and applications, underscores its emergence as a foundational standard for chiplet-based architectures. As a silicon interface IP provider working across multiple technology nodes and advancing both electrical & optical connectivity, we recognize the importance of translating real-world implementation experience into an open, scalable industry standard. UCIe 4.0 builds on this momentum, strengthening link security, enhancing in-field monitoring and serviceability, and enabling more practical deployment of high-speed, multi-die systems. These advancements further reinforce UCIe's critical role in enabling heterogeneous integration and next-generation AI & high-performance computing infrastructure.”
Saman Sadr, President & CEO, Neuron IP

Nissan Motor
“The continued evolution of vehicle intelligence requires computing architectures that are scalable and reusable across vehicle platforms and generations. Nissan believes that open and interoperable die-to-die connectivity will be a key foundation for supporting future chiplet-based SoCs in automotive applications. We welcome UCIe 4.0 as an important step toward an open, multi-vendor chiplet ecosystem. Nissan looks forward to the continued evolution of industry standards that take automotive system requirements into consideration.”
Takashi Yoshizawa, Corporate Executive, Software Defined Vehicle Engineering Division, Nissan Motor Co., Ltd.

Openchip & Software Technologies SL
"Openchip congratulates the UCIe Consortium on the release of the UCIe 4.0 specification, another milestone in turning the vision of an open, multi-vendor chiplet ecosystem into reality. At Openchip, UCIe is the interface that connects our RISC-V-based compute and AI accelerator chiplets, and UCIe 4.0 addresses exactly what large-scale AI and HPC systems demand. The new Co-optimized Profile unlocks even greater energy efficiency for tightly integrated chiplets, while Trusted Reporting of Chiplet State and secure asset provisioning establish a foundation of trust across chiplets from different vendors. As a European company building on open architectures, we see RISC-V and UCIe together as the foundation for an innovative and sovereign semiconductor ecosystem, and we are proud to contribute to the Consortium's work."
Violante Moschiano, Chief Hardware Officer, Openchip & Software Technologies SL

Qualcomm Technologies, Inc.
"The relentless demand for bandwidth density in AI infrastructure silicon is reshaping how hyperscalers build scalable systems — and UCIe-enabled chiplets are at the center of this transformation. By delivering high-performance, ultra-low-latency electrical and optical connectivity, UCIe chiplets enable tailored, scalable, and extensible solutions that dramatically compress time-to-market. The UCIe Consortium's 4.0 specification is a foundational leap — pushing bandwidth density while establishing the blueprint for the lowest-power die-to-die connections via the UCIe Co-Optimized Profile. This unlocks next-generation technologies including Co-Packaged Optics (CPO) and vertically integrated chiplets via UCIe-3D, where ultra-high throughput, ultra-low power, and tighter silicon integration are non-negotiable. At Qualcomm Technologies, we are architects of this revolution. Through close collaboration with the UCIe Consortium, customers, and ecosystem partners, we continue to expand our UCIe IP Subsystem as part of Qualcomm's End-to-End Custom Silicon portfolio — delivering chiplet connectivity solutions purpose-built for the optical I/O era."
Letizia Giuliano, Vice President of Product Management, Custom Silicon, Qualcomm Technologies, Inc.

Renesas
"Renesas is extending its leadership in automotive SoCs by building high-performance, scalable SoC solutions with chiplets. Common die-to-die interfaces are crucial to making this possible, enabling us to integrate customer solutions, broaden product offerings and shorten development cycles. As we adopt UCIe for automotive, we've recently collaborated with chiplet partners and helped incorporate a "Fail Indication" mechanism into the UCIe 4.0 specification to meet fail-safe requirements. UCIe is key to an open chiplet market, and we look forward to shaping its standardization with the UCIe Consortium and our partners."
Aish Dubey, Vice President and Head of SoC Division, High Performance Computing, Renesas

Samsung Electronics
"As the industry pushes toward increasingly sophisticated AI and HPC workloads, the need for a scalable, open interconnect has never been more critical. Through the UCIe Consortium, we are helping define a universal standard that simplifies the integration of diverse chiplets across the ecosystem. With UCIe 4.0, we are enabling even greater bandwidth and power efficiency, allowing for more complex and performant system-in-package architectures. By advancing this specification, we continue to leverage our leadership in memory and packaging to drive the future of chiplet interoperability."
Ben Hyo Gyuem Rhew, Vice President and Head of the IP Development Team, Samsung Electronics

Socionext Inc.
“As semiconductor scaling becomes increasingly challenging, heterogeneous integration and open, interoperable chiplet technologies are gaining importance. With enhanced capabilities for security, manageability, diagnostics, and reliable system operation, UCIe 4.0 represents an important step toward expanding the applicability of chiplet-based architectures to automotive and other high-reliability applications. Socionext welcomes this advancement and will continue working with the UCIe Consortium and its ecosystem partners to leverage UCIe technologies in scalable and optimized custom SoC solutions that meet the evolving needs of our customers.”
Daisuke Murakami, Executive Engineer, Global Leading Group, Socionext Inc.

Synopsis
“UCIe 4.0 marks an important step forward for the open chiplet ecosystem, enabling increasingly complex heterogeneous chiplets to operate together as complete systems. With the industry’s broadest portfolio of standards-based IP, including our silicon-proven, complete UCIe IP solution, Synopsys enables customers to implement the latest UCIe 4.0 requirements and confidently accelerate the development of secure and efficient multi-die designs for AI systems.”
Neeraj Paliwal, Senior Vice President of Product Management at Synopsys.

Toyota Motor Corporation
“Toyota welcomes the release of the UCIe 4.0 specification. Toyota believes that UCIe 4.0 represents an important step toward expanding the use of chiplet technology beyond data servers and PCs to embedded systems. By further enhancing the reliability of die-to-die communication, UCIe 4.0 is expected to accelerate the adoption of chiplet technology in automotive applications, where high levels of reliability and functional safety are essential. Toyota also expects that the continued evolution of open and interoperable industry standards will enable a diverse range of companies to participate and collaborate across industry boundaries, further advancing the global semiconductor ecosystem. Toyota believes that the continued development of this ecosystem will help enable safer, more flexible, and continuously evolving computing platforms for future mobility.”
Keiji Yamamoto, Chief Officer, Digital Information & Communication Group, Toyota Motor Corporation

Truechip
"Truechip's UCIe Verification IPs have been in use with multiple customers, covering UCIe 1.1 through UCIe 3.0. Several enhancements were incorporated in UCIe 3.0, including link robustness and manageability, runtime recalibration, priority sideband packets, and support for data rates of 48 and 64 GT/s. We are also actively working on the UCIe 4.0 VIP, which introduces new features such as TRoCS, MTP Sec and fail indication to further enhance security and reliability. It also includes UCIe Memory Access, new training setup registers, and MBTRAIN stall capabilities to improve link bring-up and debug. These new features help make UCIe the standard of choice for chiplets. We congratulate the Consortium on this milestone and appreciate its continued leadership in advancing an open and interoperable chiplet ecosystem."
Nitin Kishore, CEO, Truechip