Leaders in semiconductors, packaging, IP suppliers, foundries, and cloud service providers join forces to standardize chiplet ecosystem

Key highlights:
- Advanced Semiconductor Engineering, Inc. (ASE), AMD, Arm, Google Cloud, Intel Corporation, Meta, Microsoft Corporation, Qualcomm Incorporated, Samsung, and Taiwan Semiconductor Manufacturing Company launch new Universal Chiplet Interconnect Express (UCIe) technology to establish a chiplet ecosystem and future generations of chiplet technologies.
- UCIe 1.0 specification ratified to provide a complete standardized die-to-die interconnect with physical layer, protocol stack, software model, and compliance testing to enable end users to easily mix and match chiplet components from a multi-vendor ecosystem for System-on-Chip (SoC) construction, including customized SoC.
- New open standard establishes an open chiplet ecosystem and ubiquitous interconnect at the package level. Interested companies and institutions are encouraged to join.

Beaverton, OR, USA – March 2, 2022 – Advanced Semiconductor Engineering, Inc. (ASE), AMD, Arm, Google Cloud, Intel Corporation, Meta, Microsoft Corporation, Qualcomm Incorporated, Samsung, and Taiwan Semiconductor Manufacturing Company today announced the formation of an industry consortium that will establish a die-to-die interconnect standard and foster an open chiplet ecosystem.

The organization, representing a diverse ecosystem of market segments, will address customer requests for more customizable package-level integration, connecting best-in-class die-to-die interconnect and protocols from an interoperable, multi-vendor ecosystem.

Universal Chiplet Interconnect Express (UCIe) Specification now available
The founding companies also ratified the UCIe specification, an open industry standard developed to establish a ubiquitous interconnect at the package level. The UCIe 1.0 specification covers the die-to-die I/O physical layer, die-to-die protocols, and software stack which leverage the well-established PCI Express® (PCIe®) and Compute Express Link™ (CXL™) industry standards. The specification will be available to UCIe members and available to download on the website.

Open for membership
The founding companies represent a wide range of industry expertise and include leading cloud service providers, foundries, system OEMs, silicon IP providers, and chip designers, and they are in the process of finalizing incorporation as an open standards body. Upon incorporation of the new UCIe industry organization later this year, member companies will begin work on the next generation of UCIe technology, including defining the chiplet form factor, management, enhanced security, and other essential protocols. To learn more about membership opportunities, contact admin@UCIexpress.org.

Resources:
- Universal Chiplet Interconnect Express (UCIe) White Paper

About Universal Chiplet Interconnect Express (UCIe)

Universal Chiplet Interconnect Express (UCIe) is an open specification that defines the interconnect between chiplets within a package, enabling an open chiplet ecosystem and ubiquitous interconnect at the package level. Advanced Semiconductor Engineering, Inc. (ASE), AMD, Arm, Google Cloud, Intel Corporation, Meta, Microsoft Corporation, Qualcomm Incorporated, Samsung, and Taiwan Semiconductor Manufacturing Company are forming an open industry standard organization to promote and further develop the technology, and to establish a global ecosystem supporting chiplet design. For more information, visit www.UCIexpress.org.

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Universal Chiplet Interconnect Express (UCIe) Promoter Statements of Support (Alphabetized by Company)

Advanced Semiconductor Engineering, Inc. (ASE)
"The age of Chiplets has truly arrived, driving the industry to evolve from silicon-centric thinking to system level planning and placing crucial focus on co-design of IC and package. We are confident that UCIe will play a pivotal role in enabling ecosystem efficiencies, by lowering development time and cost through open standards for interfaces between various IPs within a multi-vendor ecosystem as well as utilization of advanced package level interconnect. There is broad industry recognition that Heterogeneous Integration will help bring Chiplet-based designs to market. Given ASE's expertise in packaging, assembly, and interconnect platform technology, we will provide UCIe with meaningful perspective to ensure forthcoming standards are practicable, complemented by commercially viable performance and manufacturing costs for package level manufacturing."
Dr. Lihong Cao, Director of Engineering and Technical Marketing at ASE, Inc.

AMD
"AMD is proud to continue our long history of supporting industry standards that can enable innovative solutions addressing the evolving needs of our customers. We have been a leader in chiplet technology and welcome a multi-vendor chiplet ecosystem to enable customizable third-party integration. The UCIe standard will be a key factor to drive systems innovation leveraging heterogeneous compute engines and accelerators that will enable the best solutions optimized for performance, cost, and power efficiency."
Mark Papermaster, Executive Vice President and Chief Technology Officer, AMD

Arm
"Interoperability is essential to removing fragmentation across the Arm ecosystem, and across the industry. By collaborating with other leaders in computing, Arm is committed to helping develop standards and specifications like UCIe to enable the system designs of our future."
Andy Rose, Chief System Architect and Fellow, Arm

Google Cloud
"An open, standards based chiplet ecosystem is an important enabler to foster Systems on Chip (SoC) designs as the integration point for an optimized system. Google Cloud is pleased to contribute to the Universal Chiplet Interconnect Express standard in service of the development of a multi-vendor inter-operable chiplet marketplace for the benefit of the industry."
Partha Ranganathan, Google Fellow and Vice President

Intel Corporation
"Integrating multiple chiplets in a package to deliver product innovation across market segments is the future of the semiconductor industry and a pillar of Intel's IDM 2.0 strategy. Critical to this future is an open chiplet ecosystem with key industry partners working together under the UCIe Consortium toward a common goal of transforming the way the industry delivers new products and continues to deliver on the promise of Moore's Law."
Sandra Rivera, Executive Vice President, Intel Corporation and GM, Data Center & AI

Meta
"Meta is excited to join UCIe as a founding member to enable and foster a standards-based die-to-die interconnect. Meta initiated ecosystem development to promote chiplet-based SOCs via the Open Compute Project (OCP) and is pleased to collaborate with other industry leaders via UCIe consortium for the ongoing and future success in this area."
Vijay Rao, Directory of Technology and Strategy, Meta

Microsoft Corporation
"Microsoft is joining the UCIe industry organization to accelerate the pace of datacenter innovation and enable new breakthroughs in silicon design. We look forward to combining efforts of the organization with our own achievements to drive step-function improvements in silicon architecture for the benefit of our customers."
Dr. Leendert van Doorn, Distinguished Engineer, Azure, Microsoft

Qualcomm Incorporated
"Qualcomm is pleased that the industry is coming together to form UCIe, which should move chiplet technology forward—an important technology to address the challenges in our increasingly complex semiconductor systems."
Dr. Edward Tiedemann, Senior Vice-President, Engineering, Qualcomm Technologies, Inc.

Samsung
"Samsung envisions chiplet technology becoming necessary for performance gains in computing systems as process nodes continue to scale, with dies inside each package eventually communicating through a single language. We expect the UCIe Consortium to foster a vibrant chiplet ecosystem and establish the framework for a viable open-standard interface industry-wide. As a total solutions provider for memory, logic, and foundry, Samsung anticipates spearheading consortium efforts to further identify the best ways for enhancing system performance through chiplet technology."
Cheolmin Park, Vice President of Memory Product Planning Team at Samsung Electronics

Taiwan Semiconductor Manufacturing Company

"TSMC is pleased to participate in this industry-wide consortium that will broaden the eco-system for package-level integration. TSMC offers various silicon and packaging technologies that provide multiple implementation options for heterogeneous UCIe devices."

Lee-Chung Lu, TSMC Fellow and Vice President of Design and Technology Platform