# The UCIe™ 1.1 Specification: Future Applications of Chiplets

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Chairman of UCIe Consortium

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# Meet the Presenter

Dr. Debendra Das Sharma

Intel Senior Fellow and co-GM Memory and I/O Technologies, Intel Corporation

UCIe Consortium Chairman

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# Agenda

- UCIe Overview
- UCIe: An Open Standard for Chiplets
- Introducing UCIe 1.1
- UCIe – Usage Models
- Future Directions and Conclusions



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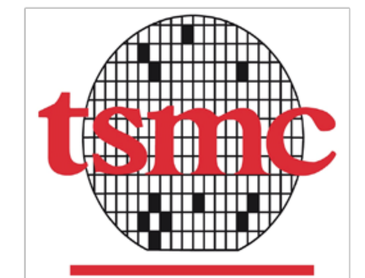
UCIe™
Universal Chiplet
Interconnect Express

130+ Member Companies and growing!

# Board Members

Leaders in semiconductors, packaging, IP suppliers, foundries, and cloud service providers are joining together to drive
The open chiplet ecosystem.

JOIN US!

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# UCIe Consortium is Open for Membership

- UCIe Consortium welcomes interested companies and institutions to join the organization at the **Contributor and Adopter level.**

- **UCIe** was founded in March 2022, incorporated in June 2022. Two levels of memberships: Contributor and Adopter

- **Contributor Membership**
  - Access the Final Specifications (ex: 1.0, 1.1, 2.0, etc.)
  - Implement with the IP protections as outlined in the Agreements
  - Right to attend Corporation trade shows or other industry events as determined by the Board
  - Participate in the technical working groups
  - Influence the direction of the technology
  - Access the intermediate (dot level) specifications
  - Election to get to the Promoter Class/ Board every year when the term of half the board completes

- **Adopter Membership**
  - Access the Final Specifications (ex: 1.0, 1.1, 2.0, etc.), but not intermediate level specifications
  - Implement with the IP protections as outlined in the Agreements
  - Right to attend Corporation trade shows or other industry events as determined by the Board

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# Universal Chiplet Interconnect Express (UCIe):

# An Open Standard for Chiplets

Guiding principles of UCIe

1. Open Ecosystem with Plug-and-play
2. Backward compatible evolution when appropriate to ensure investment protection
3. Best power, performance, and cost metrics across the industry applicable across the entire compute continuum
4. Continuously innovate to meet the needs of evolving compute landscape

(Leveraging decades of experience driving successful industry standards at the board level: PCIe, CXL, USB, etc.)

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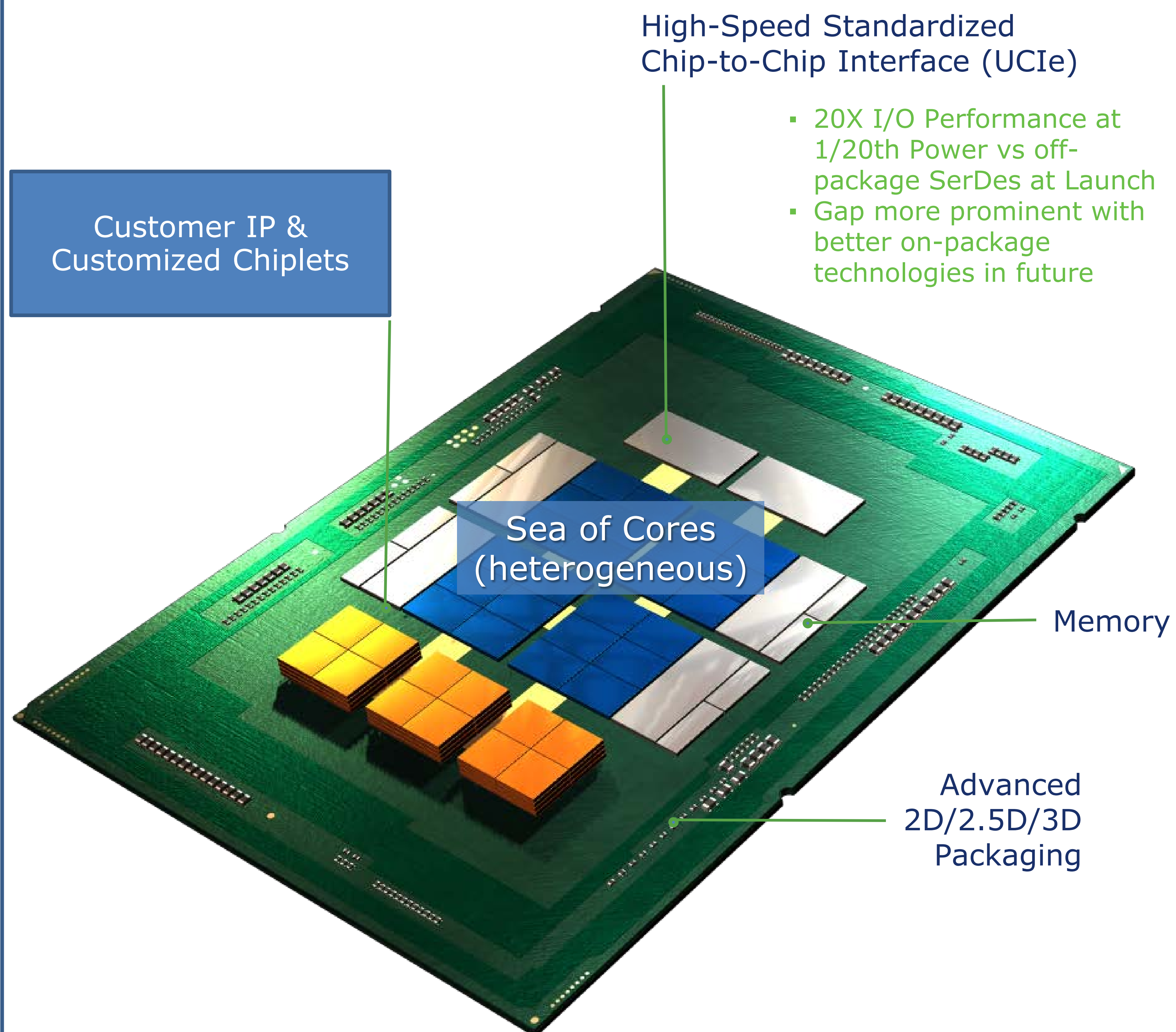
# Motivation




Heterogeneous Integration Fueled by an Open Chiplet Ecosystem
(Mix-and-match chiplets from different process nodes / fabs / companies / assembly)

## Align Industry around an open platform to enable chiplet based solutions

- Enables construction of SoCs that exceed maximum reticle size
  - Package becomes new System-on-a-Chip (SoC) with same dies (Scale Up)
- Reduces time-to-solution (e.g., enables die reuse)
- Lowers portfolio cost (product & project)
  - Enables optimal process technologies
  - Smaller (better yield)
  - Reduces IP porting costs
  - Lowers product SKU cost
- Enables a customizable, standard-based product for specific use cases (bespoke solutions)
- Scales innovation (manufacturing/ process locked IPs)

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# Key Metrics and Adoption Criteria

## Key Technology Metrics

- Bandwidth density (linear & area)
  - Data Rate & Bump Pitch
- Energy Efficiency (pJ/b)
  - Scalable energy consumption
  - Low idle power (entry/exit time)
- Latency (end-to-end: Tx+Rx)
- Channel Reach
- Technology, frequency, & BER
- Reliability & Availability
- Cost (Standard vs advanced packaging)

## Factors Affecting Wide Adoption

- Interoperability
- Full-stack, plug-and-play with existing s/w is+
- Different usages/segments
- Technology
  - Across process nodes & packaging options
  - Power delivery & cooling
  - Repair strategy (failure/yield improvement)
  - Debug – controllability & observability
- Broad industry support / Open ecosystem
  - Learnings from other standards efforts

UCIe - Architected and specified from the ground-up to deliver the best KPIs while meeting wide adoption criteria to drive innovations at package level

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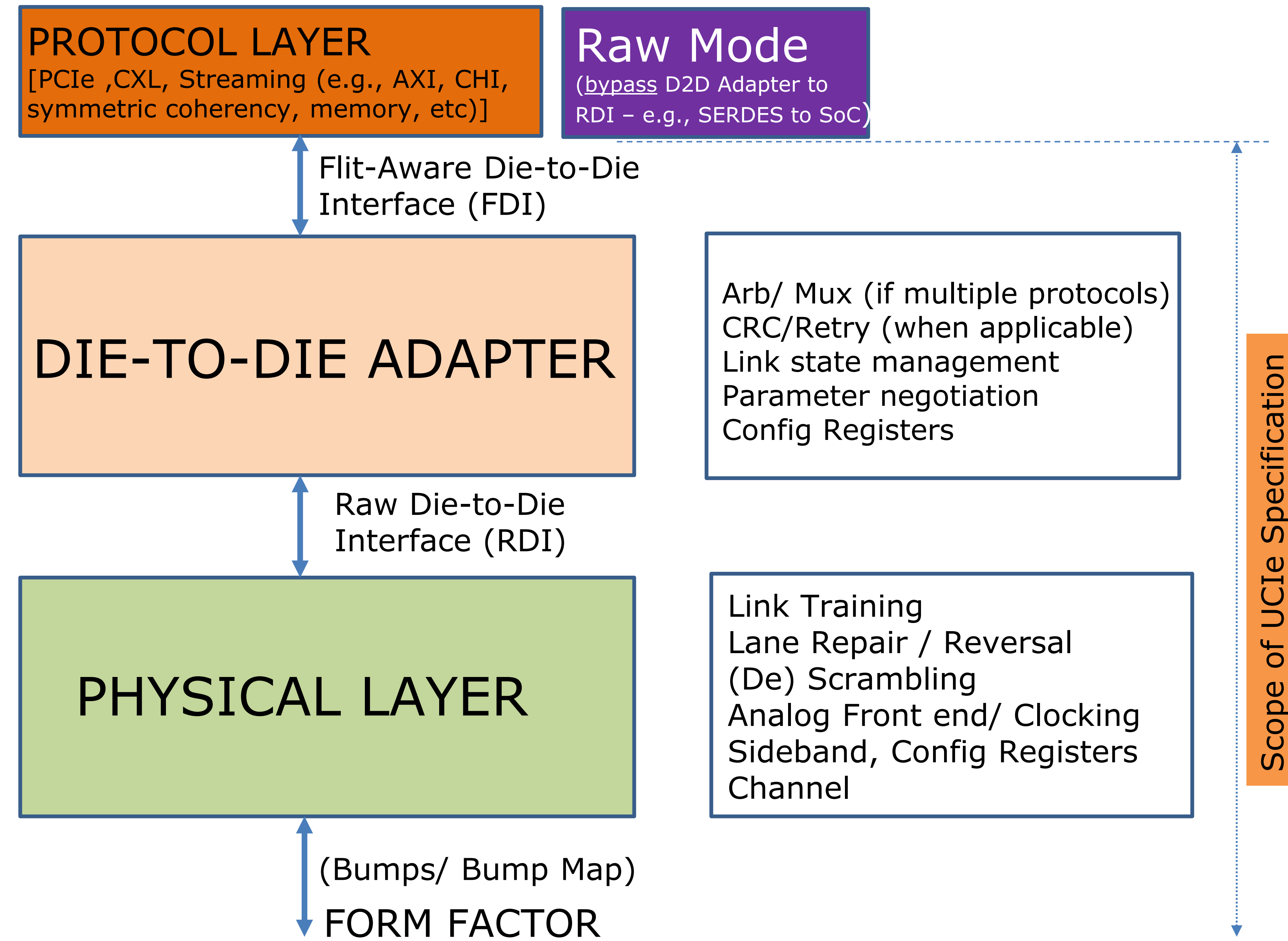
# UCIe 1.0 Specification

- **Layered Approach with industry-leading KPIs**
- **Physical Layer:** Die-to-Die I/O
- **Die to Die Adapter:** Reliable delivery
  - Support for multiple protocols: bypassed in raw mode
- **Protocol:** CXL/PCIe and Streaming
  - **CXL™/PCIe® for volume attach and plug-and-play**
    - SoC construction issues are addressed w/ CXL/PCIe
    - CXL/PCIe addresses common use cases
      - I/O attach, Memory, Accelerator
  - **Streaming for other protocols**
    - Scale-up (e.g., CPU/ GP-GPU/Switch from smaller dies)
    - Protocol can be anything (e.g., AXI/CHI/SFI/CPI/ etc)
    - Raw Mode only
- **Well defined specification**: interoperability and future evolution
  - Configuration register for discovery and run-time
    - control and status reporting in each layer
    - transparent to existing drivers
  - Form-factor and Management
  - Compliance for interoperability
  - Plug-and-play IPs with RDI/ FDI interface

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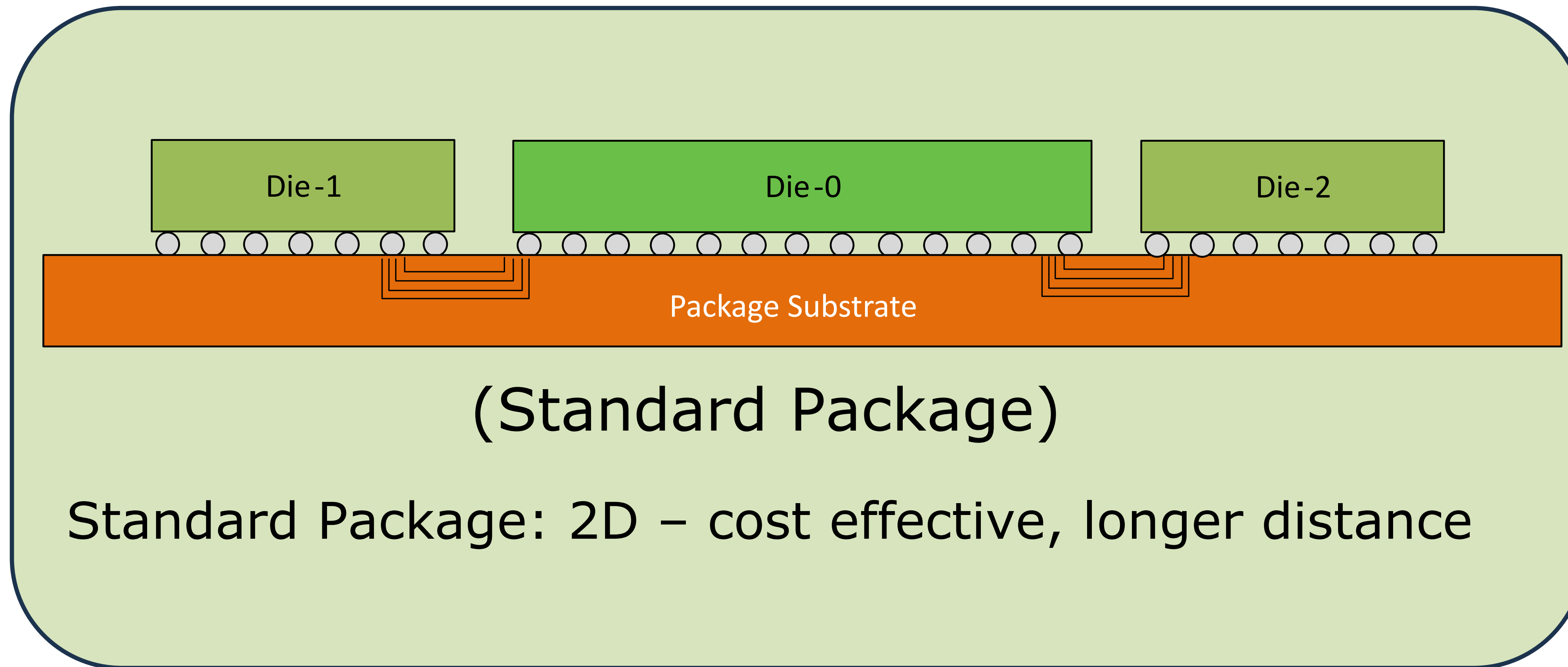
# UCIe 1.0: Supports Standard and Advanced Packages

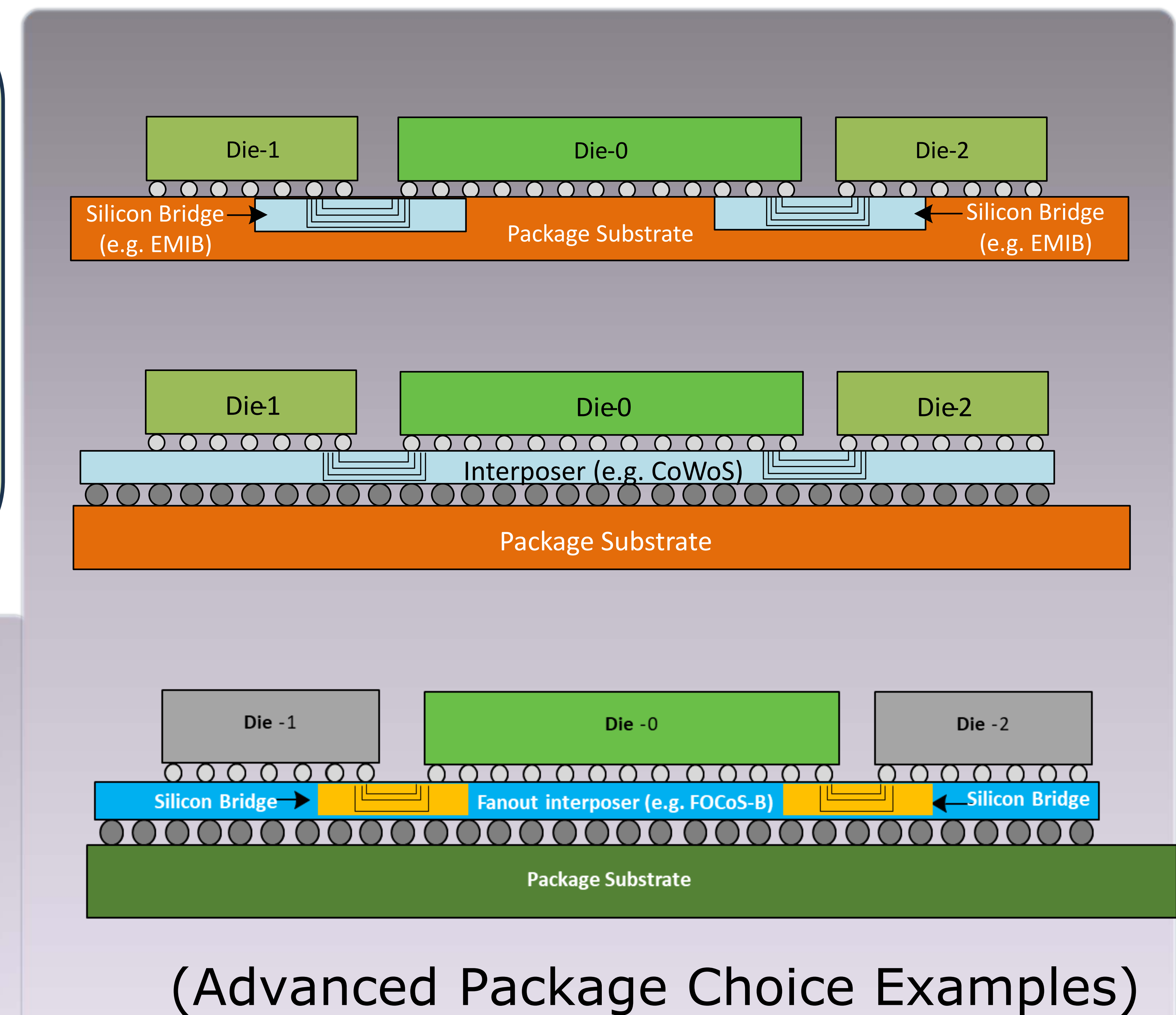



(Standard Package)

Standard Package: 2D – cost effective, longer distance

**Advanced Packages**: 2.5D – power-efficient, high bandwidth density

Dies can be manufactured anywhere and assembled anywhere – can mix 2D and 2.5D in same package – Flexibility for SoC designer




(Advanced Package Choice Examples)

One UCIe 1.0 spec supports **different flavors** of packaging options to build an open ecosystem

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# UCIe PHY: Bump-out for Interoperability

- UCIe architected with process portability in mind
  - Circuit components can be built with common digital/ analog structures
- Bump-out specified in the specification for interoperability even with future bump-pitch reductions
  - Die rotation and mirroring supported

| | txdatasb | | txcksb | | vccaon | | vccaon | | rxcksb | | rxdatasb |
|---|---|---|---|---|---|---|---|---|---|---|---|
| vccio | | vccio | | vccio | | vccio | | vccio | | vccio | |
| | vss | | vss | | vccio | | vss | | vss | | vss |
| vss | | txdata7 | | txdata9 | | vss | | rxdata8 | | rxdata6 | |
| | txdata5 | | txckn | | txdata11 | | rxdata10 | | rxckp | | rxdata4 |
| vss | | txdata6 | | txdata8 | | vss | | rxdata9 | | rxdata7 | |
| | txdata4 | | txckp | | txdata10 | | rxdata11 | | rxckn | | rxdata5 |
| vccio | | vss | | vss | | vccio | | vss | | vss | |
| | txdata1 | | txvld | | txdata15 | | rxdata14 | | rxtrk | | rxdata0 |
| vccio | | txdata3 | | txdata13 | | vccio | | rxdata12 | | rxdata2 | |
| | txdata0 | | txtrk | | txdata14 | | rxdata15 | | rxvld | | rxdata1 |
| vss | | txdata2 | | txdata12 | | vss | | rxdata13 | | rxdata3 | |

(UCIe-S Unstacked Bump-out)

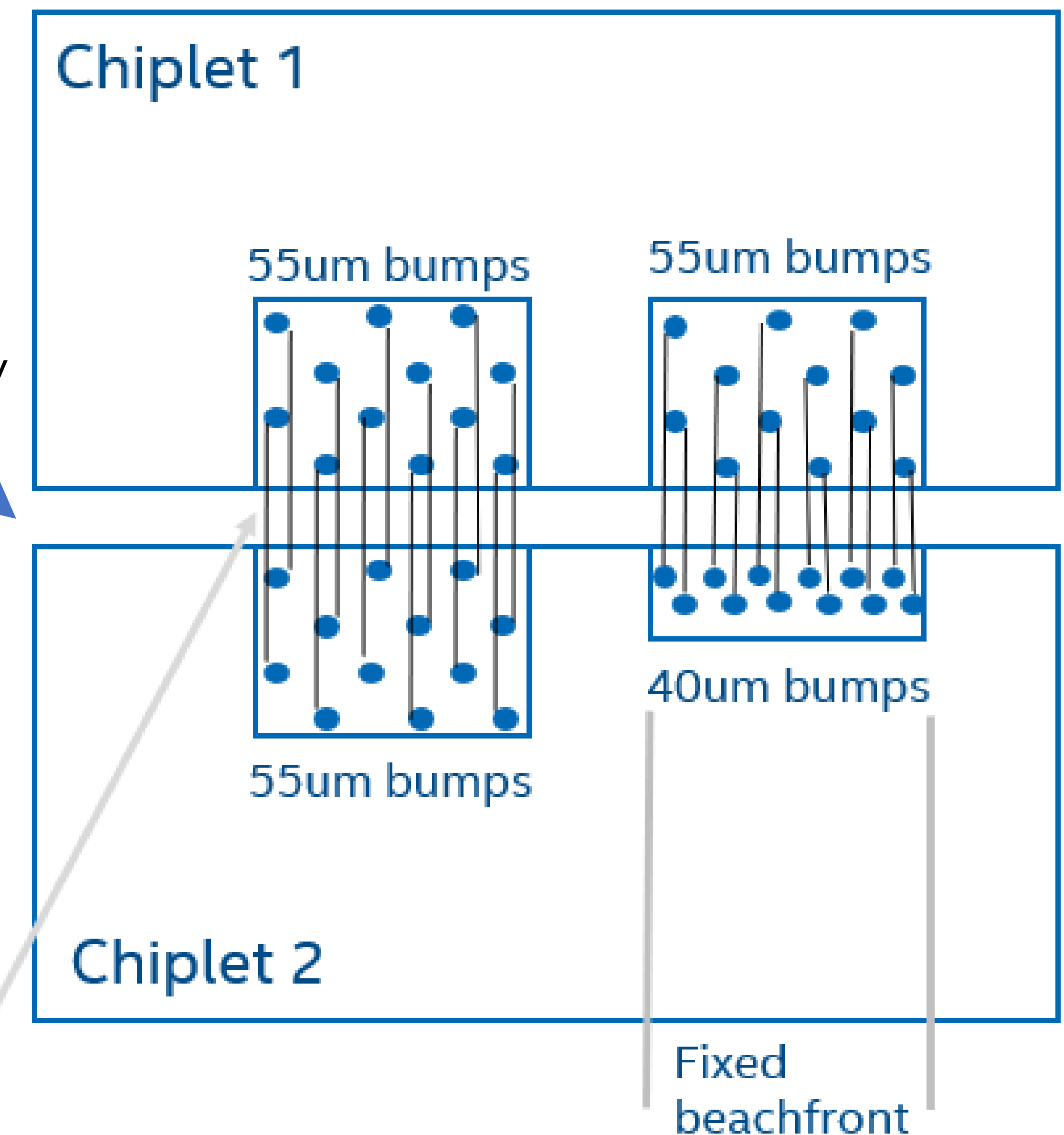
| | m2rxdatasb | | m2rxcksb | | vccaon | | m2txcksb | | m2txdatasb | | vccaon |
|---|---|---|---|---|---|---|---|---|---|---|---|
| m1txdatasb | | m1txcksb | | vccaon | | vccaon | | m1rxcksb | | m1rxdatasb | |
| | vccio | | vccio | | vccio | | vccio | | vccio | | vccio |
| vss | | vss | | vss | | vss | | vss | | vss | |
| | m2rxdata6 | | m2rxdata8 | | vss | | m2txdata9 | | m2txdata7 | | vss |
| m2rxdata4 | | m2rxckp | | m2rxdata10 | | m2txdata11 | | m2txckn | | m2txdata5 | |
| | m2rxdata7 | | m2rxdata9 | | vss | | m2txdata8 | | m2txdata6 | | vss |
| m2rxdata5 | | m2rxckn | | m2rxdata11 | | m2txdata10 | | m2txckp | | m2txdata4 | |
| | vss | | vss | | vss | | vss | | vss | | vss |
| m2rxdata0 | | m2rxtrk | | m2rxdata14 | | m2txdata15 | | m2txvld | | m2txdata1 | |
| | m2rxdata2 | | m2rxdata12 | | vss | | m2txdata13 | | m2txdata3 | | vss |
| m2rxdata1 | | m2rxvld | | m2rxdata15 | | m2txdata14 | | m2txtrk | | m2txdata0 | |
| | m2rxdata3 | | m2rxdata13 | | vccio | | m2txdata12 | | m2txdata2 | | vccio |
| vccio | | vccio | | vccio | | vccio | | vccio | | vccio | |
| | vss | | vss | | vccio | | vss | | vss | | vccio |
| vss | | m1txdata7 | | m1txdata9 | | vss | | m1rxdata8 | | m1rxdata6 | |
| | m1txdata5 | | m1txckn | | m1txdata11 | | m1rxdata10 | | m1rxckp | | m1rxdata4 |
| vss | | m1txdata6 | | m1txdata8 | | vss | | m1rxdata9 | | m1rxdata7 | |
| | m1txdata4 | | m1txckp | | m1txdata10 | | m1rxdata11 | | m1rxckn | | m1rxdata5 |
| vccio | | vss | | vss | | vccio | | vss | | vss | |
| | m1txdata1 | | m1txvld | | m1txdata15 | | m1rxdata14 | | m1rxtrk | | m1rxdata0 |
| vccio | | m1txdata3 | | m1txdata13 | | vccio | | m1rxdata12 | | m1rxdata2 | |
| | m1txdata0 | | m1txtrk | | m1txdata14 | | m1rxdata15 | | m1rxvld | | m1rxdata1 |
| vss | | m1txdata2 | | m1txdata12 | | vss | | m1rxdata13 | | m1rxdata3 | |

(UCIe-S Stacked Bump-out)

Fixed beachfront allows for
Multi-generational compatibility
As bump pitches decrease

| | rxcksbRD | | rxcksb | | vccio | | rxdatasb | | rxdatasbRD |
|---|---|---|---|---|---|---|---|---|---|
| txdatasbRD | | txdatasb | | vccio | | txcksb | | txcksbRD | |
| | rxdata50 | | rxdata35 | | rxdata29 | | rxdata14 | | rxdataRD0 |
| rxdataRD3 | | rxdata49 | | rxdata34 | | rxdata28 | | rxdata13 | |
| | rxdata51 | | rxdata36 | | rxdata30 | | rxdata15 | | vss |
| rxdata63 | | vccio | | rxdata33 | | vccio | | rxdata12 | |
| | rxdata52 | | vss | | rxdata31 | | vss | | rxdata0 |
| vss | | rxdata48 | | rxdata32 | | rxdata27 | | rxdata11 | |
| | rxdata53 | | rxdata37 | | rxdataRD1 | | rxdata16 | | rxdata1 |
| rxdata62 | | rxdata47 | | rxdataRD2 | | rxdata26 | | rxdata10 | |
| | rxdata54 | | rxdata38 | | vss | | rxdata17 | | vss |
| rxdata61 | | rxdata46 | | vccio | | rxdata25 | | rxdata9 | |
| | rxdata55 | | rxdata39 | | rxckRD | | rxdata18 | | rxdata2 |
| vss | | rxdata45 | | rxvldRD | | rxdata24 | | rxdata8 | |
| | rxdata56 | | vss | | rxckn | | rxdata19 | | rxdata3 |
| rxdata60 | | rxdata44 | | rxvld | | vss | | rxdata7 | |
| | rxdata57 | | rxdata40 | | rxckp | | rxdata20 | | vss |
| rxdata59 | | rxdata43 | | rxtrk | | rxdata23 | | rxdata6 | |
| | rxdata58 | | rxdata41 | | vss | | rxdata21 | | rxdata4 |
| vss | | rxdata42 | | vccio | | rxdata22 | | rxdata5 | |
| | vccio | | vccio | | vccio | | vccio | | vccio |
| vccio | | txdata21 | | vccio | | txdata41 | | txdata58 | |
| | txdata5 | | txdata22 | | vss | | txdata42 | | vss |
| txdata4 | | txdata20 | | txckp | | txdata40 | | txdata57 | |
| | txdata6 | | txdata23 | | txtrk | | txdata43 | | txdata59 |
| vss | | txdata19 | | txckn | | vss | | txdata56 | |
| | txdata7 | | vss | | txvld | | txdata44 | | txdata60 |
| txdata3 | | txdata18 | | txckRD | | txdata39 | | txdata55 | |
| | txdata8 | | txdata24 | | txvldRD | | txdata45 | | vss |
| txdata2 | | txdata17 | | vccio | | txdata38 | | txdata54 | |
| | txdata9 | | txdata25 | | vss | | txdata46 | | txdata61 |
| vccio | | vccio | | vccio | | vccio | | vccio | |
| | txdata10 | | txdata26 | | txdataRD2 | | txdata47 | | txdata62 |
| txdata1 | | txdata16 | | txdataRD1 | | txdata37 | | txdata53 | |
| | txdata11 | | txdata27 | | txdata32 | | txdata48 | | vss |
| txdata0 | | vss | | txdata31 | | vss | | txdata52 | |
| | txdata12 | | vss | | txdata33 | | vss | | txdata63 |
| vss | | txdata15 | | txdata30 | | txdata36 | | txdata51 | |
| | txdata13 | | txdata28 | | txdata34 | | txdata49 | | txdataRD3 |
| txdataRD0 | | txdata14 | | txdata29 | | txdata35 | | txdata50 | |
| | vccio | | vccio | | vccio | | vccio | | vccio |
| vccio | | vccio | | vccio | | vccio | | vccio | |

(UCIe-A Bump-out)




CoWos or EMIB or FoCoS or similar tight-pitch tech

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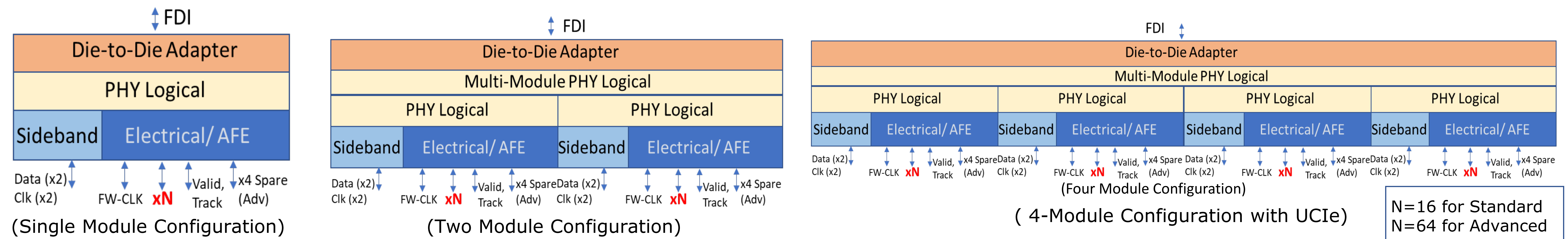
# Physical Layer

- Unit is One Module: uni-directional: 1, 2, or 4 modules form a Link
  - 16 (64) SE Lanes for Std (Adv)
  - 1 SE Lane of valid
  - 1 differential pair of forwarded clock
  - 1 lane (SE) calibration - Track
  - Lane reversal on Transmit side
  - Reliability: Spare Lanes in Adv; degradation in Std
  - Supported frequencies: 4, 8, 12, 16, 24, 32 GHz
  - A component must support all data rates up to its advertised maximum data rate for interoperability
  - B/W per module/ dir: 64 GB/s Std, 256 GB/s Adv: Two module gets 2X, 4-module gets 4X
- Sideband: always on; 2 Lanes/ direction @ 800 MHz – data and clock
  - Used for training, debug, management, etc; Leverages depopulated bumps to ensure no extra shore-line
- Valid used for effective dynamic power management

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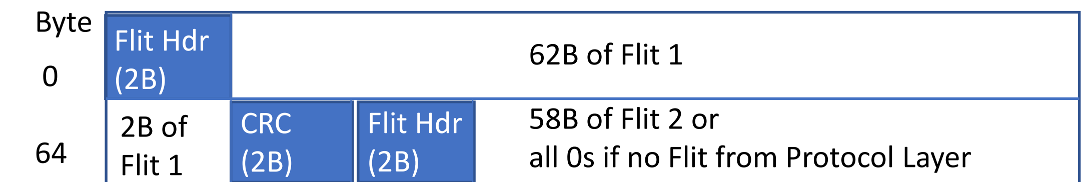
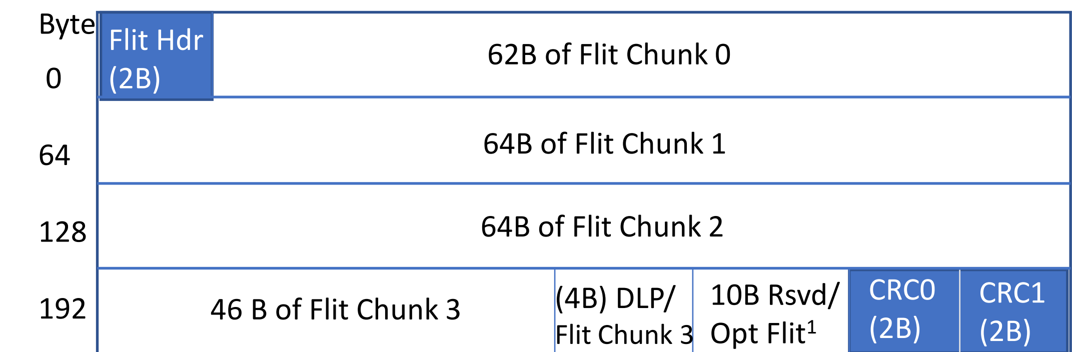
# D2D Adapter and Flit Mapping through FDI

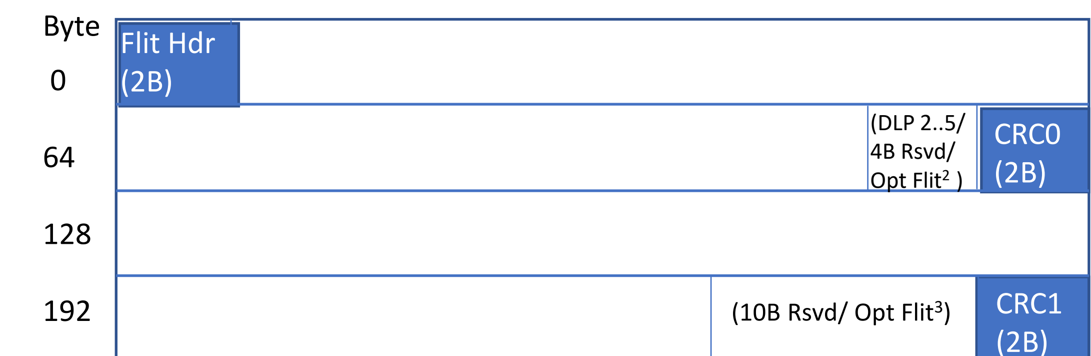
- Responsible for packetization
  - Adds Flit Header (2B) and CRC (2B)
- Supported Flit Sizes: 68B and two flavors of 256B
  - Decided at negotiation
- Flit Hdr (2B): Protocol ID (3b), Credit (1b), Flit Ack/Nak management (2b command + 8b sequence number), Rsvd (2b)
- CRC: Covers 128B payload (smaller payloads are 0-extended)
  - Triple bit flip detection guarantee with 16 bits
  - Replay if CRC fails
  - Sample RTL code for CRC provided in the spec




(a. 68-Byte Flit – usage CXL 2.0/ PCIe Non-Flit Mode/ Streaming)




(b. 256-Byte Flit – usage CXL 3.0/ PCIe 6.0)




(c. 256-Byte Latency-Optimized Flit – usage CXL 3.0/ Streaming)

(Opt Flit is for better link efficiency to use the unused CRC/ FEC bytes in PCIe/ CXL)

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# Introducing UCIe 1.1

Enhancements for **Automotive Segment** Usage

**New Usages**: Streaming Protocols with Full Stack

Cost Optimization for **Advanced Packaging**

Enhancements for **Compliance Testing**

UCIe 1.1 is Fully Backward Compatible with UCIe 1.0

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# UCIe 1.1: Automotive Enhancements

- Automotive is an important segment of the compute continuum – Announcing the formation of an Automotive WG to explore enhancing UCIe for automotive usages
- Automotive moving towards UCIe based chiplets to leverage the broad ecosystem
- UCIe is a compelling technology for automotive compute needs. UCIe 1.1 has the following enhancements building on UCIe 1.0:
  - Preventive Monitoring for link health
  - Run-time testability of failure rate of the link
  - Field repairability to get around faults

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# UCIe 1.1: Automotive Enhancements

- Preventive Monitoring:
  - Added new registers to capture Eye Margin (eye width and eye height, if applicable) information in a standard format from training
  - SW can trigger periodic retrain of the link to get eye margin info using existing UCIe 1.0 mechanism
- Run-time Testability of Link Health
  - Existing mechanism in UCIe 1.0: Periodic parity Flit injection and checking for monitoring health of each Lane in mission mode
  - Enhancements in UCIe 1.1: Per-Lane error Log/ counter with ability to send interrupt
  - Usage: Software can inject periodic parity Flit and monitor the UCIe 1.1 error log register to assess the health of each Lane to assess the Link health and repair if needed
- Field Repairability
  - Already present with UCIe 1.0 (mask Lane, retrain, etc) – so no changes in this area
- We will continue to monitor and meet the automotive needs

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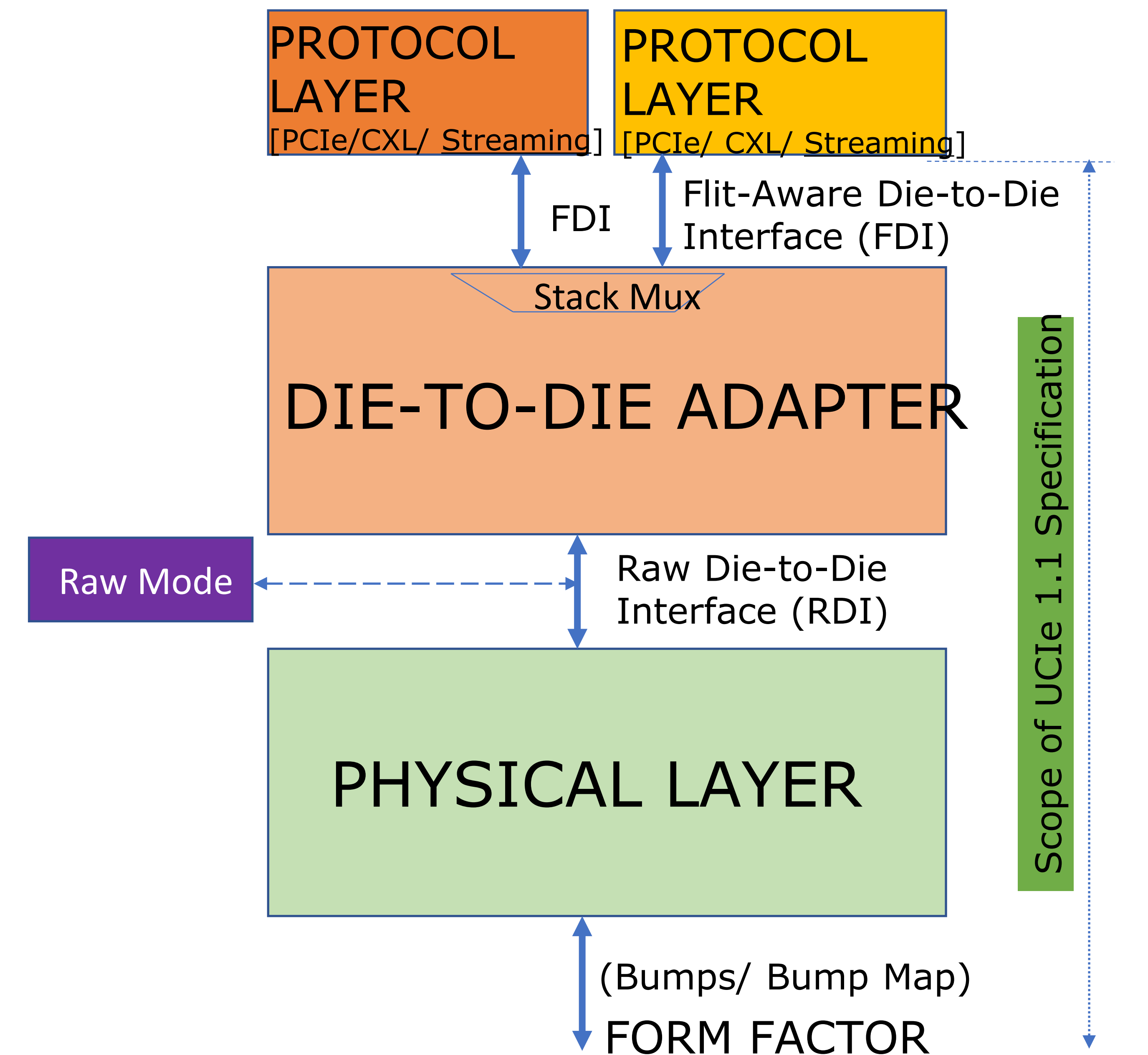
# UCIe 1.1: Streaming Protocols on Full Stack

- UCIe 1.0 supports Streaming Protocol (e.g., AXI, CHI, SMP coherency protocols, SFI, CPI) only in Raw Mode
- Two enhancements with UCIe 1.1 (raw mode still supported)
  1. Streaming Protocols can use the D2D adapter
     - Enables them to reuse the CRC, Retry etc.
     - Mechanism: map streaming to existing Flit Formats at FDI interface
  2. Streaming Protocols can multiplex with other protocols with on-demand interleaving
     - Enables co-existence of multiple protocols (e.g., streaming for processing, PCIe for discovery, DMA, TLB, error reporting, interrupt, etc.) for different use cases
     - Mechanism: Protocol muxing for Streaming protocol with existing Flit Formats at FDI interface

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# UCIe 1.1: Streaming Protocol Flit Formats

| Format Number | Flit Format Name | PCIe Non-Flit Mode | PCIe Flit Mode | CXL 68B Flit Mode | CXL 256B Flit Mode | Streaming | |
|---|---|---|---|---|---|---|---|
| | | | | | | UCIe 1.0 | UCIe 1.1 |
| 1 | Raw | Optional | Optional | Optional | Optional | Mandatory | |
| 2 | 68B | Mandatory | N/A | Mandatory | N/A | N/A | Supported |
| 3 | Standard 256B End Header | N/A | Mandatory | N/A | N/A | N/A | Supported |
| 4 | Standard 256B Start Header | N/A | Optional | N/A | Mandatory | N/A | Supported |
| 5 | Latency Optimized 256B without optional bytes | N/A | N/A | N/A | Optional | N/A | Supported |
| 6 | Latency Optimized 256B with optional bytes | N/A | Strongly Recommended | N/A | Strongly Recommended | N/A | Supported |

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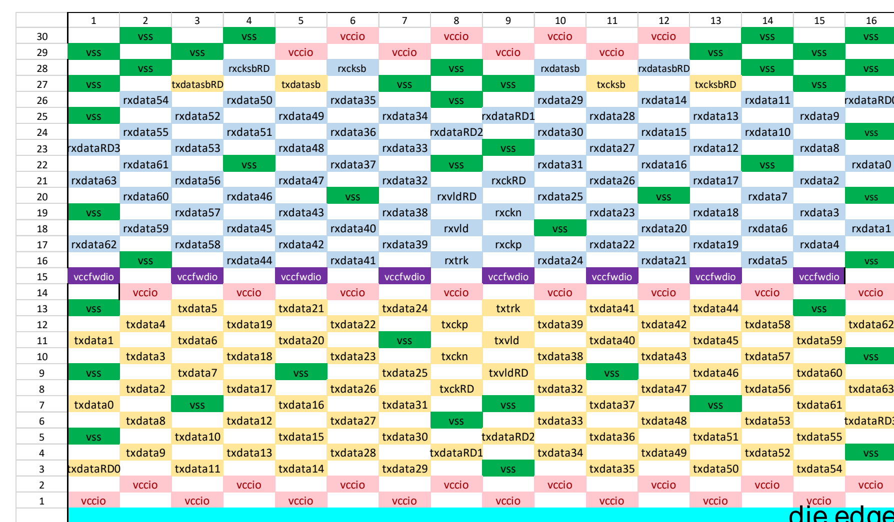
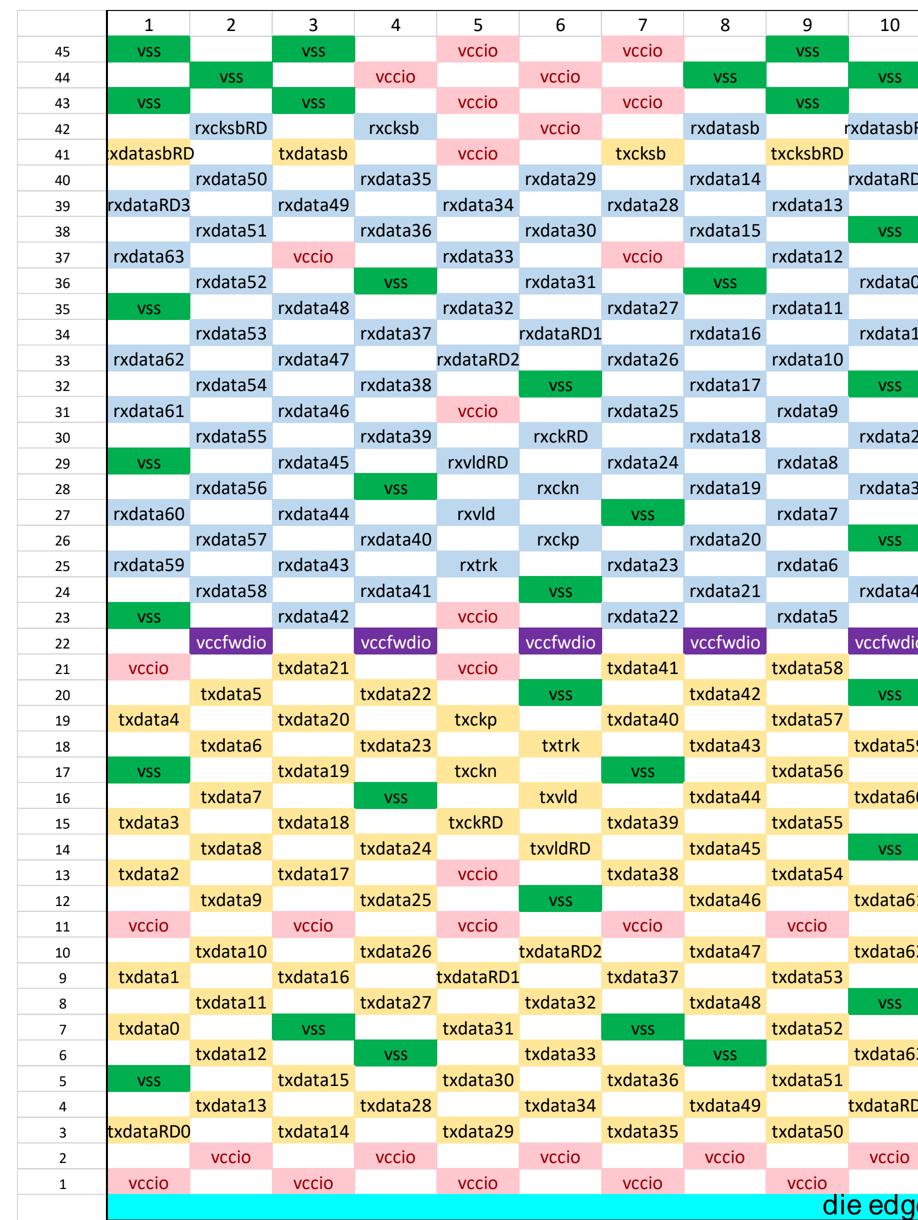
# UCIe-A Bump Map Optimization

- Two newly introduced bumpout configurations for maintaining optimized BW/mm^2 across allowable bump pitch range
  - Existing bumpout : 10-column
  - New: 8-column, 16-column
  - Suggested usage guideline:

| BP | Max Data Rate by Spec | Columns within 388.8 shoreline |
|---|---|---|
| 25-30 | 12 | 16 |
| 31-37 | 16 | |
| 38-44 | 24 | 10 |
| 45-50 | 32 | |
| 51-55 | 32 | 8 |



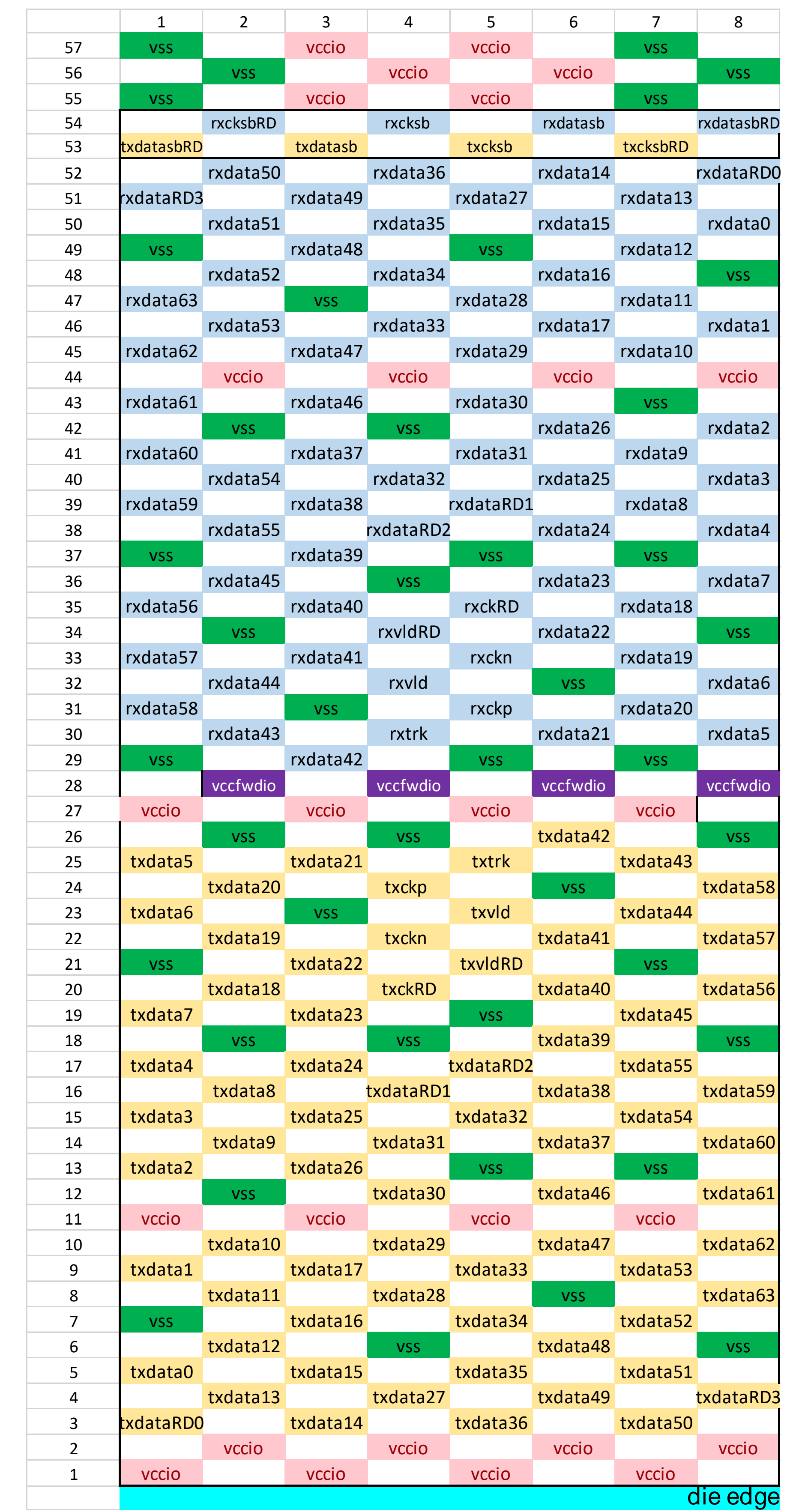
**16Col**
Recommended for
25-37um bump pitch



| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|---|---|---|---|---|---|---|---|---|---|
| 45 | vss | | vss | | vccio | | vccio | | vss | |
| 44 | | vss | | vccio | | vccio | | vss | | vss |
| 43 | vss | | vss | | vccio | | vccio | | vss | |
| 42 | | rxcksbRD | | rxcksb | | vccio | | rxdatasb | | rxdatasbRD |
| 41 | txdatasbRD | | txdatasb | | vccio | | txcksb | | txcksbRD | |
| 40 | | rxdata50 | | rxdata35 | | rxdata29 | | rxdata14 | | rxdataRD0 |
| 39 | rxdataRD3 | | rxdata49 | | rxdata34 | | rxdata28 | | rxdata13 | |
| 38 | | rxdata51 | | rxdata36 | | rxdata30 | | rxdata15 | | vss |
| 37 | rxdata63 | | vccio | | rxdata33 | | vccio | | rxdata12 | |
| 36 | | rxdata52 | | vss | | rxdata31 | | vss | | rxdata0 |
| 35 | vss | | rxdata48 | | rxdata32 | | rxdata27 | | rxdata11 | |
| 34 | | rxdata53 | | rxdata37 | | rxdataRD1 | | rxdata16 | | rxdata1 |
| 33 | rxdata62 | | rxdata47 | | rxdataRD2 | | rxdata26 | | rxdata10 | |
| 32 | | rxdata54 | | rxdata38 | | vss | | rxdata17 | | vss |
| 31 | rxdata61 | | rxdata46 | | vccio | | rxdata25 | | rxdata9 | |
| 30 | | rxdata55 | | rxdata39 | | rxckRD | | rxdata18 | | rxdata2 |
| 29 | vss | | rxdata45 | | rxvldRD | | rxdata24 | | rxdata8 | |
| 28 | | rxdata56 | | vss | | rxckn | | rxdata19 | | rxdata3 |
| 27 | rxdata60 | | rxdata44 | | rxvld | | vss | | rxdata7 | |
| 26 | | rxdata57 | | rxdata40 | | rxckp | | rxdata20 | | vss |
| 25 | rxdata59 | | rxdata43 | | rxtrk | | rxdata23 | | rxdata6 | |
| 24 | | rxdata58 | | rxdata41 | | vss | | rxdata21 | | rxdata4 |
| 23 | vss | | rxdata42 | | vccio | | rxdata22 | | rxdata5 | |
| 22 | | vccfwdio | | vccfwdio | | vccfwdio | | vccfwdio | | vccfwdio |
| 21 | vccio | | txdata21 | | vccio | | txdata41 | | txdata58 | |
| 20 | | txdata5 | | txdata22 | | vss | | txdata42 | | vss |
| 19 | txdata4 | | txdata20 | | txckp | | txdata40 | | txdata57 | |
| 18 | | txdata6 | | txdata23 | | txtrk | | txdata43 | | txdata59 |
| 17 | vss | | txdata19 | | txckn | | vss | | txdata56 | |
| 16 | | txdata7 | | vss | | txvld | | txdata44 | | txdata60 |
| 15 | txdata3 | | txdata18 | | txckRD | | txdata39 | | txdata55 | |
| 14 | | txdata8 | | txdata24 | | txvldRD | | txdata45 | | vss |
| 13 | txdata2 | | txdata17 | | vccio | | txdata38 | | txdata54 | |
| 12 | | txdata9 | | txdata25 | | vss | | txdata46 | | txdata61 |
| 11 | vccio | | vccio | | vccio | | vccio | | vccio | |
| 10 | | txdata10 | | txdata26 | | txdataRD2 | | txdata47 | | txdata62 |
| 9 | txdata1 | | txdata16 | | txdataRD1 | | txdata37 | | txdata53 | |
| 8 | | txdata11 | | txdata27 | | txdata32 | | txdata48 | | vss |
| 7 | txdata0 | | vss | | txdata31 | | vss | | txdata52 | |
| 6 | | txdata12 | | vss | | txdata33 | | vss | | txdata63 |
| 5 | vss | | txdata15 | | txdata30 | | txdata36 | | txdata51 | |
| 4 | | txdata13 | | txdata28 | | txdata34 | | txdata49 | | txdataRD3 |
| 3 | txdataRD0 | | txdata14 | | txdata29 | | txdata35 | | txdata50 | |
| 2 | | vccio | | vccio | | vccio | | vccio | | vccio |
| 1 | vccio | | vccio | | vccio | | vccio | | vccio | |

die edge

**10Col** (in spec 1.0)
Recommended for
38-50um bump pitch



| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| 57 | vss | | vccio | | vccio | | vss | |
| 56 | | vss | | vccio | | vccio | | vss |
| 55 | vss | | vccio | | vccio | | vss | |
| 54 | | rxcksbRD | | rxcksb | | rxdatasb | | rxdatasbRD |
| 53 | txdatasbRD | | txdatasb | | txcksb | | txcksbRD | |
| 52 | | rxdata50 | | rxdata36 | | rxdata14 | | rxdataRD0 |
| 51 | rxdataRD3 | | rxdata49 | | rxdata27 | | rxdata13 | |
| 50 | | rxdata51 | | rxdata35 | | rxdata15 | | rxdata0 |
| 49 | vss | | rxdata48 | | vss | | rxdata12 | |
| 48 | | rxdata52 | | rxdata34 | | rxdata16 | | vss |
| 47 | rxdata63 | | vss | | rxdata28 | | rxdata11 | |
| 46 | | rxdata53 | | rxdata33 | | rxdata17 | | rxdata1 |
| 45 | rxdata62 | | rxdata47 | | rxdata29 | | rxdata10 | |
| 44 | | vccio | | vccio | | vccio | | vccio |
| 43 | rxdata61 | | rxdata46 | | rxdata30 | | vss | |
| 42 | | vss | | vss | | rxdata26 | | rxdata2 |
| 41 | rxdata60 | | rxdata37 | | rxdata31 | | rxdata9 | |
| 40 | | rxdata54 | | rxdata32 | | rxdata25 | | rxdata3 |
| 39 | rxdata59 | | rxdata38 | | rxdataRD1 | | rxdata8 | |
| 38 | | rxdata55 | | rxdataRD2 | | rxdata24 | | rxdata4 |
| 37 | vss | | rxdata39 | | vss | | vss | |
| 36 | | rxdata45 | | vss | | rxdata23 | | rxdata7 |
| 35 | rxdata56 | | rxdata40 | | rxckRD | | rxdata18 | |
| 34 | | vss | | rxvldRD | | rxdata22 | | vss |
| 33 | rxdata57 | | rxdata41 | | rxckn | | rxdata19 | |
| 32 | | rxdata44 | | rxvld | | vss | | rxdata6 |
| 31 | rxdata58 | | vss | | rxckp | | rxdata20 | |
| 30 | | rxdata43 | | rxtrk | | rxdata21 | | rxdata5 |
| 29 | vss | | rxdata42 | | vss | | vss | |
| 28 | | vccfwdio | | vccfwdio | | vccfwdio | | vccfwdio |
| 27 | vccio | | vccio | | vccio | | vccio | |
| 26 | | vss | | vss | | txdata42 | | vss |
| 25 | txdata5 | | txdata21 | | txtrk | | txdata43 | |
| 24 | | txdata20 | | txckp | | vss | | txdata58 |
| 23 | txdata6 | | vss | | txvld | | txdata44 | |
| 22 | | txdata19 | | txckn | | txdata41 | | txdata57 |
| 21 | vss | | txdata22 | | txvldRD | | vss | |
| 20 | | txdata18 | | txckRD | | txdata40 | | txdata56 |
| 19 | txdata7 | | txdata23 | | vss | | txdata45 | |
| 18 | | vss | | vss | | txdata39 | | vss |
| 17 | txdata4 | | txdata24 | | txdataRD2 | | txdata55 | |
| 16 | | txdata8 | | txdataRD1 | | txdata38 | | txdata59 |
| 15 | txdata3 | | txdata25 | | txdata32 | | txdata54 | |
| 14 | | txdata9 | | txdata31 | | txdata37 | | txdata60 |
| 13 | txdata2 | | txdata26 | | vss | | vss | |
| 12 | | vss | | txdata30 | | txdata46 | | txdata61 |
| 11 | vccio | | vccio | | vccio | | vccio | |
| 10 | | txdata10 | | txdata29 | | txdata47 | | txdata62 |
| 9 | txdata1 | | txdata17 | | txdata33 | | txdata53 | |
| 8 | | txdata11 | | txdata28 | | vss | | txdata63 |
| 7 | vss | | txdata16 | | txdata34 | | txdata52 | |
| 6 | | txdata12 | | vss | | txdata48 | | vss |
| 5 | txdata0 | | txdata15 | | txdata35 | | txdata51 | |
| 4 | | txdata13 | | txdata27 | | txdata49 | | txdataRD3 |
| 3 | txdataRD0 | | txdata14 | | txdata36 | | txdata50 | |
| 2 | | vccio | | vccio | | vccio | | vccio |
| 1 | vccio | | vccio | | vccio | | vccio | |

die edge

**8Col**
Recommended for
51-55um bump pitch

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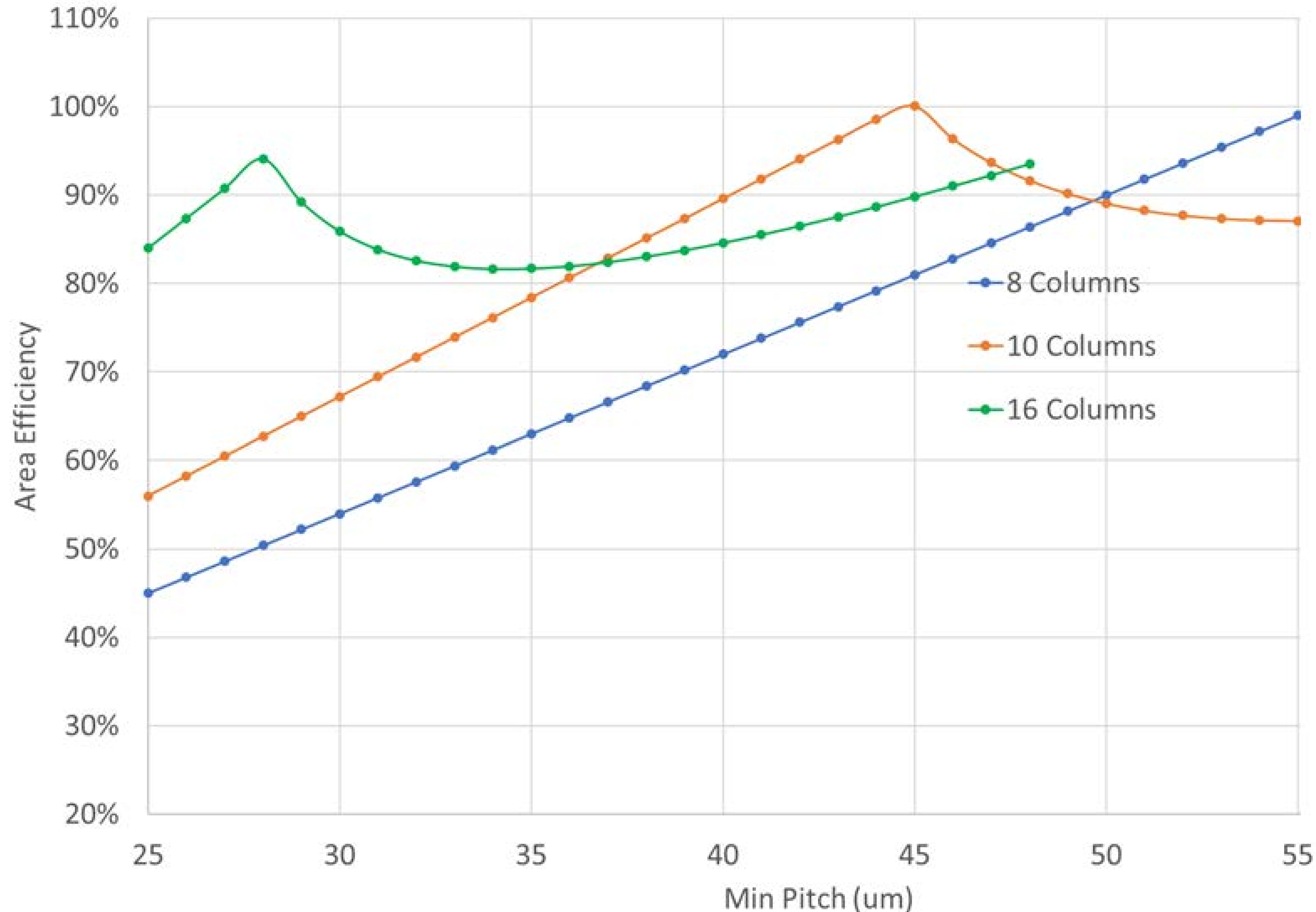
# UCIe-A Area/Column Type Efficiency Plots




- Points of overlap are the optimal cross-over points between recommended 8/10/16-column bump maps
- At the lower bump pitch range, >80% area efficiency is acceptable given overall magnitude of PHY depth is lower
- As bump pitch increases, >90% area efficiency is desired due to the much bigger PHY depth (um)
  - Example: 10% of 1000um is greater than 20% of 400um

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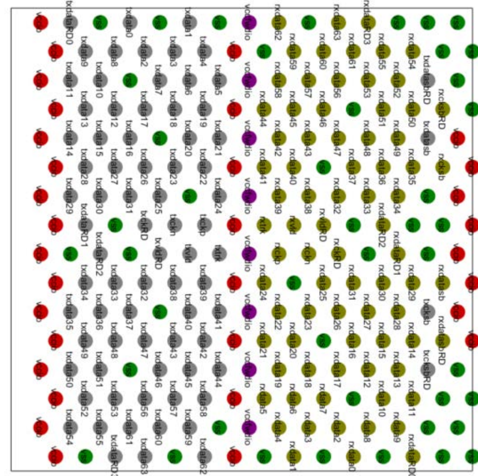
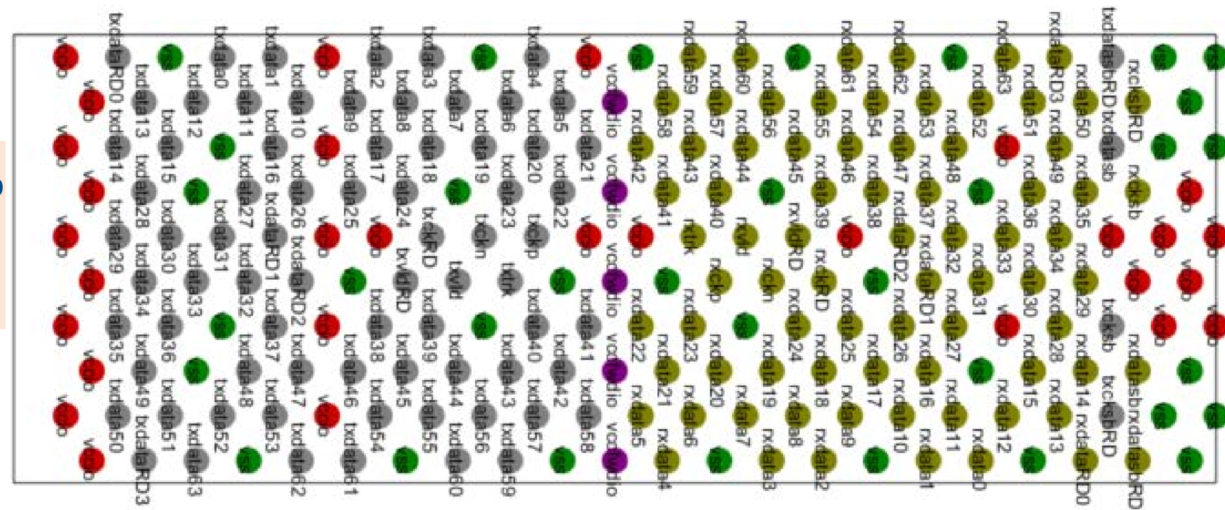
# Physical Illustration x64 Bump Maps



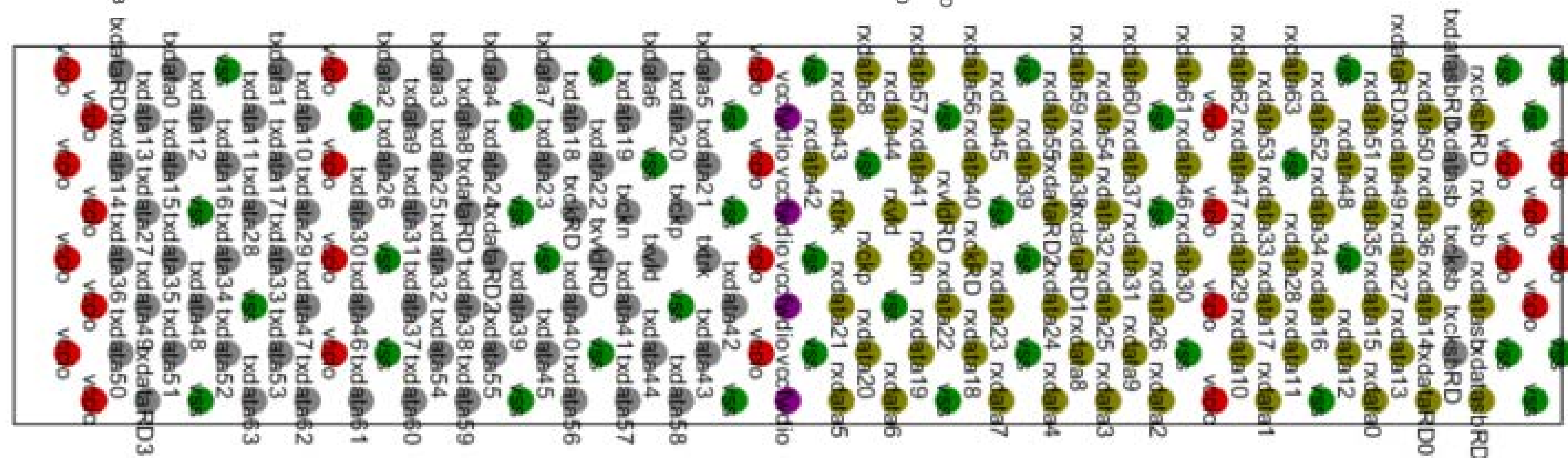
16-Col at 25 µm pitch
388.8 µm shoreline
~388 µm depth

die edge



10-Col at 45 µm pitch
388.8 µm shoreline
~1043 µm depth

<u>In UCIe 1.0 spec: No change</u>



8-Col at 55 µm pitch
388.8 µm shoreline
~1585 µm depth

Note: Die bottom view looking at the micro bumps. The orientation is only for illustration purpose. The "die edge" shown on the left can be any of the four edges of a die.

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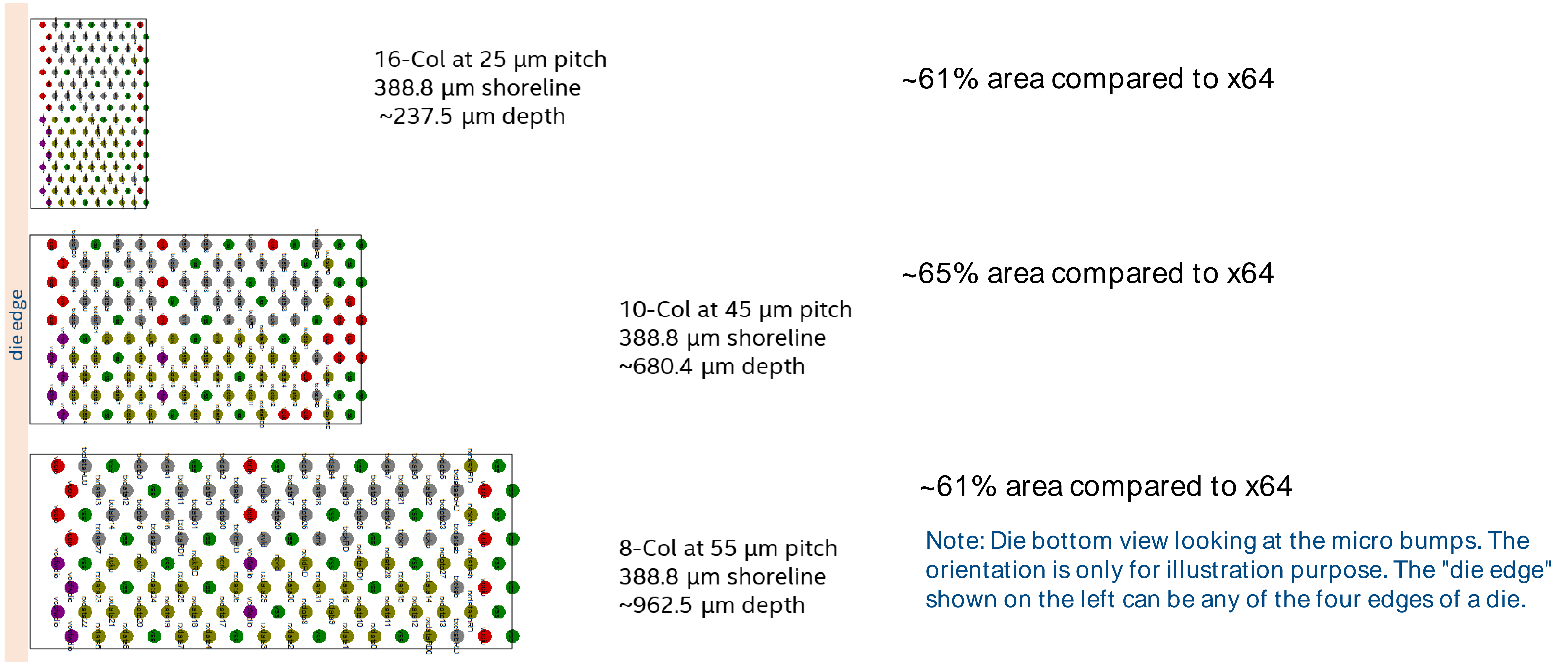
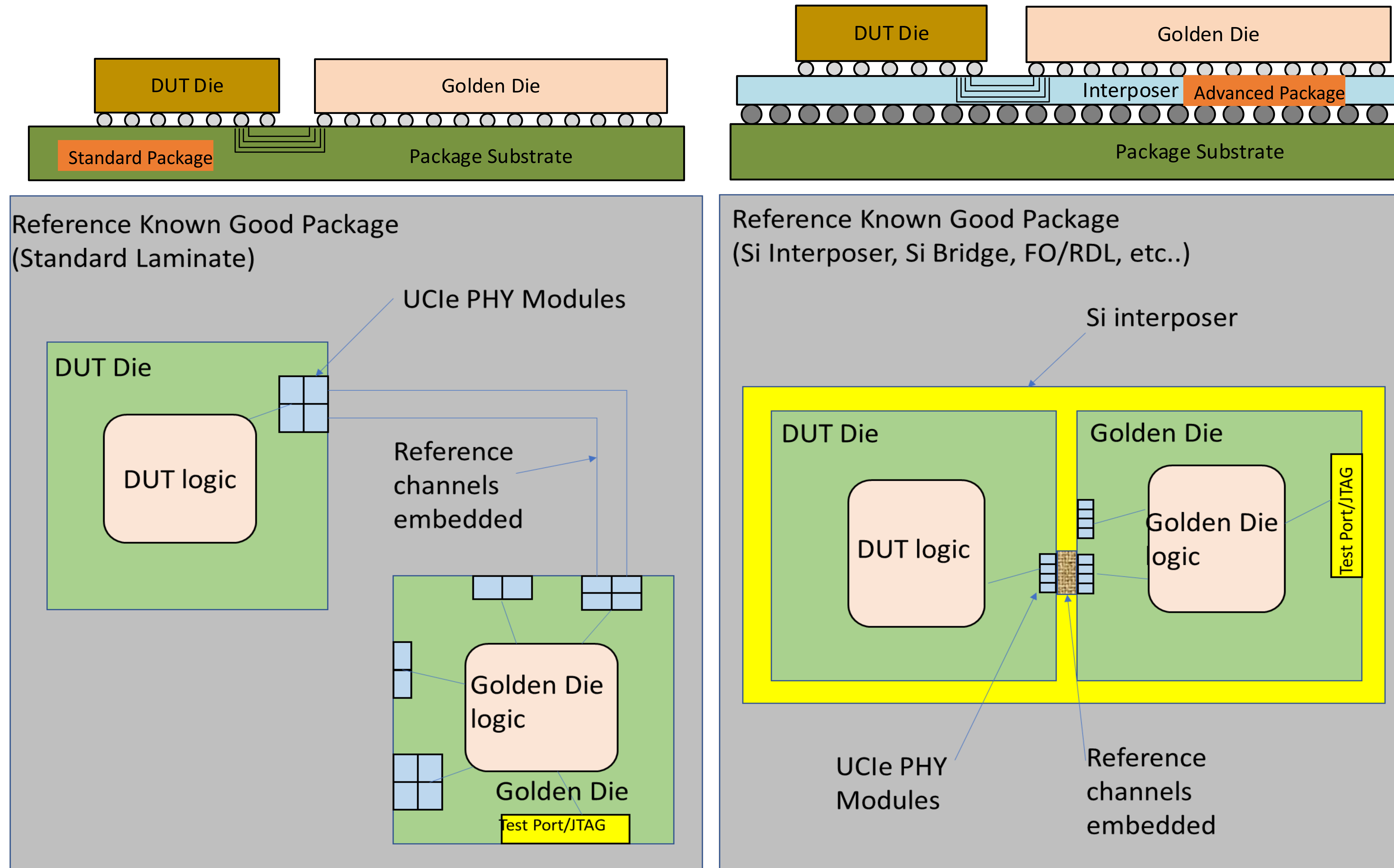
# UCIe 1.1: Reduced Width for Cost Optimization

- Some usages need x32 width native width in addition to x64 (e.g., FPGAs with lots of parallel narrower widths consistent with processing capability). One can not gang-up these x32s though (that would be x64s)
- x64 can interoperate with a x32 by utilizing only the lower 32 lanes per module




X32 enables lower-cost advanced packaging by allowing single layer routing in addition silicon area reduction by ~40%

# UCIe Compliance: Setup




Ingredients: Reference known good package with Reference Channels, Golden Die, DUT

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# UCIe 1.1 Enhancements: Compliance

- PHY Level Compliance:
  - Timing/ Voltage margin, BER measurement, Lane to lane skew, Even/Odd eye asymmetry, Tx EQ – register based control
  - Golden die: all above plus ability to inject errors/ cause timeouts in various phases of training
- D2D Adapter Compliance:
  - DUT: Register based injection of NOP/Test Flit, Replay etc.
  - Golden Die: Support all formats, ability to inject the above, error in sideband, etc.
- Protocol Compliance: Expected to be orchestrated through an FPGA / dedicated silicon connected to the golden die
  - Leverage PCIe and CXL protocol compliance as defined by those specifications
  - Streaming Protocols: Use their respective compliance

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# UCIe Usage Models

UCIe™
Universal Chiplet
Interconnect Express

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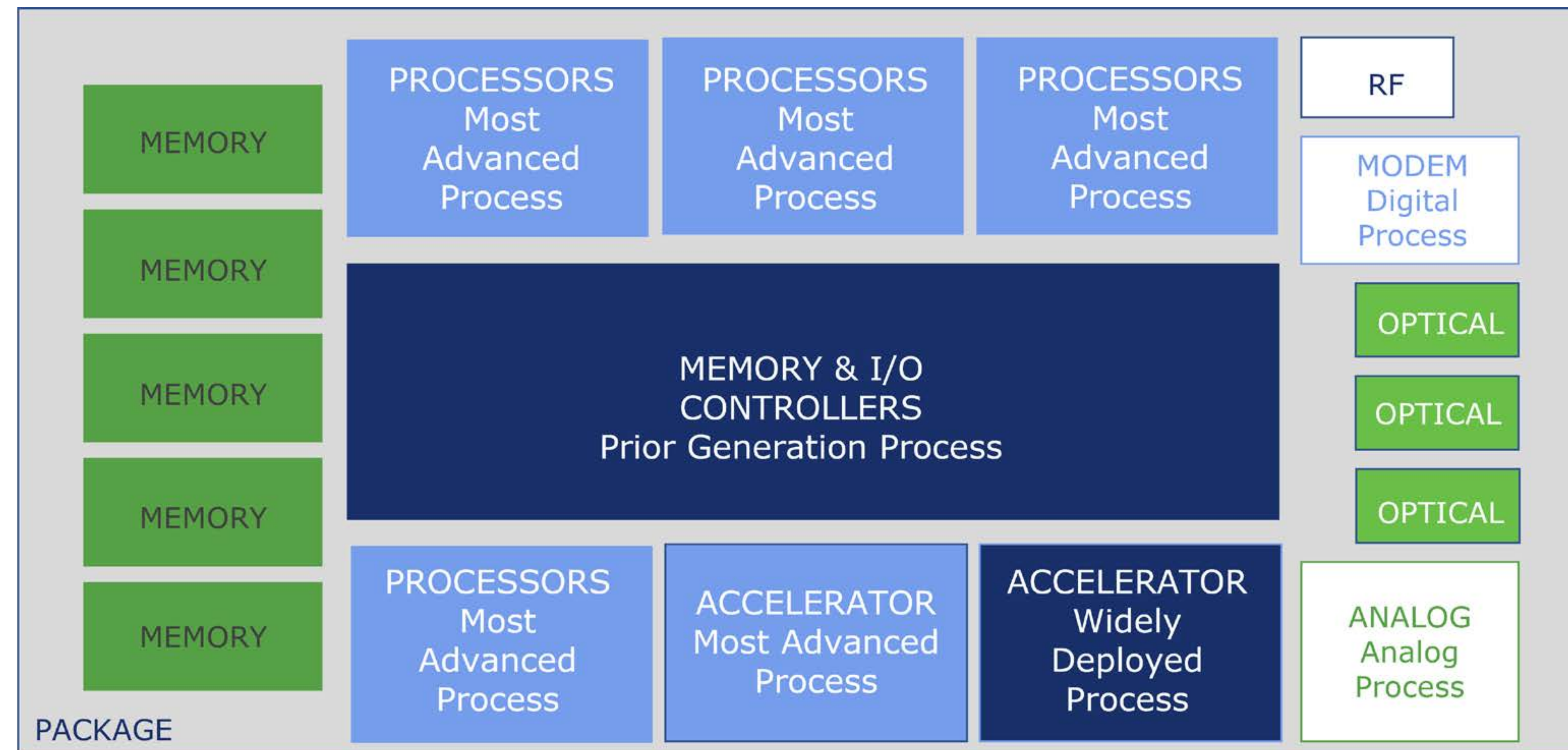
# Usage Models for UCIe: SoC at Package level

- SoC as a Package level construct
  - Standard and/ or Advanced package
  - Homogeneous and/or heterogeneous chiplets
  - Mix and match chiplets from multiple suppliers
- Across segments: Hand-held, Client, Server, Workstation, Comms, HPC, Automotive, IoT, etc.
- UCIe PHY and D2D adapter common
  - PCIe/CXL protocol for plug-and-play
  - Streaming for others (similar to board level connectivity today where scale-up systems are on PCIe PHY)
  - Similar to PCIe/ CXL at board level




Processors: symmetric coherency protocol mapped on UCIe through FDI
Memory: CXL.Mem mapped on UCIe through FDI
Accelerators: PCIe/ CXL mapped on UCIe through FDI
Modem/ RF/ Optical: Raw mode on UCIe

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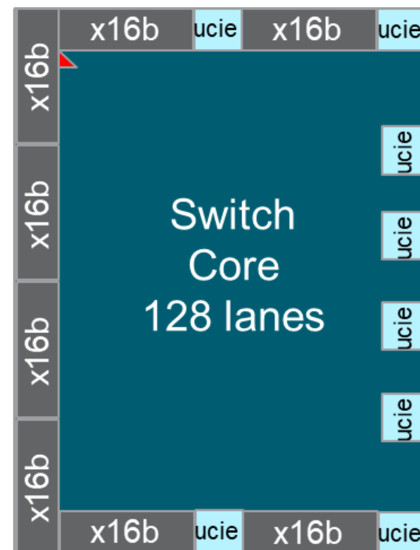
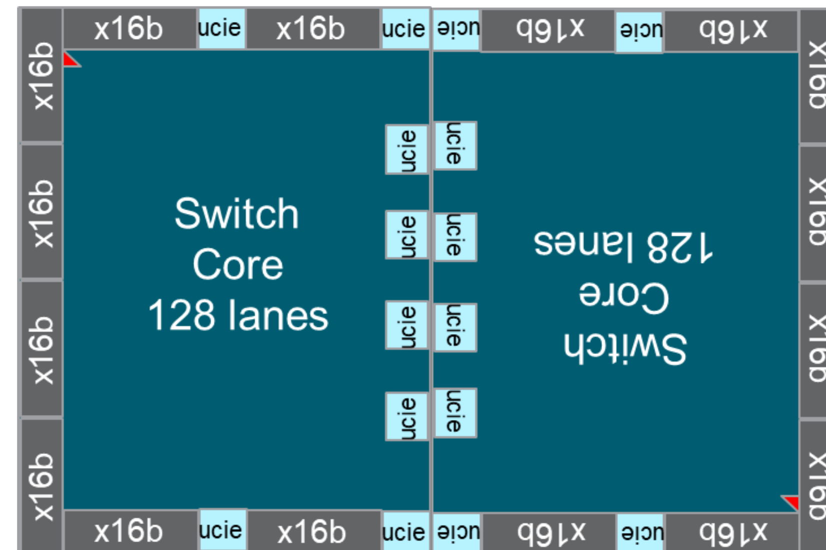
# Example Scale-up SoC from Homogeneous Dies: Large Switch with On-Die Protocol as Streaming Over UCIe

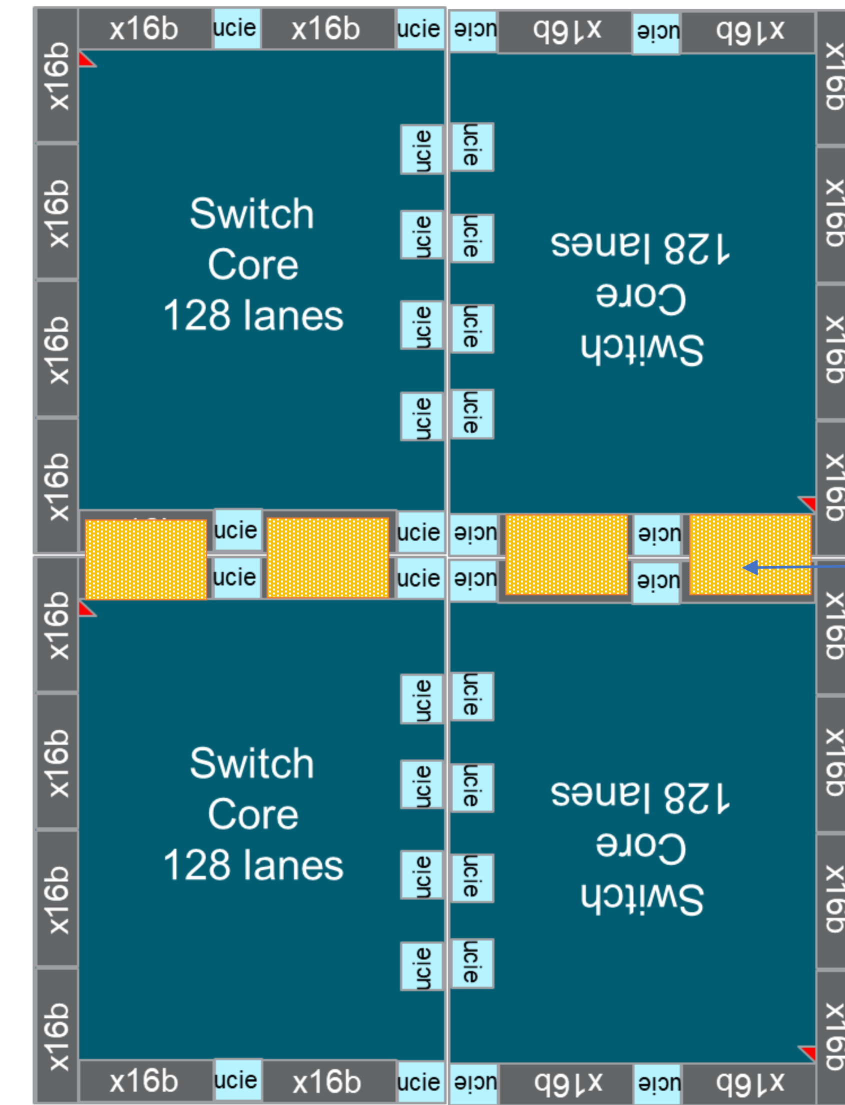
- Need large radix CXL switches – challenges: reticle limit, cost, etc.
- UCIe based Chiplets should help with scalable products
- 64G Gen6 x16b CXL links
- UCIe as d2d interconnect – while this is a scale-up CXL switch , a switch vendor may prefer to have their on-die interconnect protocol be transported over UCIe rather than create a hierarchy of switches which will not work for CXL 2.0 tree-based topology



Small CXL Switch (128 lanes)



Medium-sized CXL Switch (256 lanes)



Large CXL switch (512 lanes)

One can construct CPUs (low, medium, large core-count CPUs) from smaller dies connected through UCIe using the same principle
Here the UCIe PHY and D2D adapter will carry the packetized version of internal CPU interconnect fabric

Ack: Nathan Kalyanasundaram

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# Example Scale-up Package using Streaming and Open-Plug-In using PCIe/ CXL

Compute
CPU CPU CPU
CPU CPU CPU
CHI interconnect
Memory controller
UCIe
D2D adapter
PHY

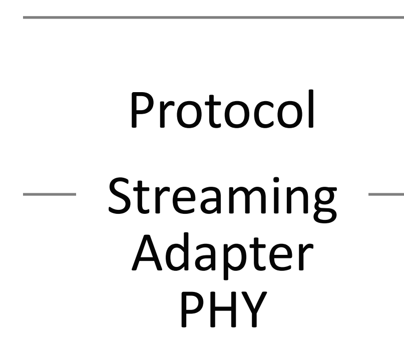
Compute
CPU CPU CPU
CPU CPU CPU
UCIe
PHY
D2D Adapter
CHI interconnect
Memory controller
CHI/CXL
UCIe
D2D Adapter
PHY

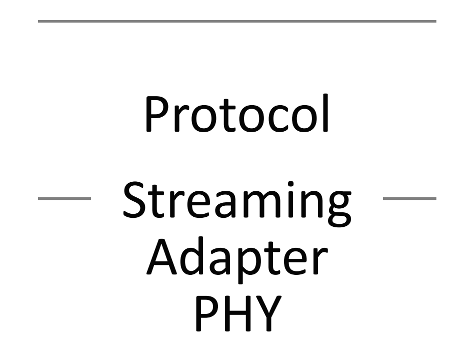
Acceleration
Accelerators
UCIe
PHY
D2D Adapter
CHI/CXL
Internal (e.g., CHI) interconnect
Mem controller

(3 dies on one package)

Not drawn to scale

- Transporting the same on-chip protocol allows seamless use of architecture specific features without protocol conversion
- Streaming interface with additional flit formats provide link robustness using UCIe defined data-link CRC and retry






- Any device type in this open plug-in slot with CXL (or CHI if both support it)

Ack: Marvin Denman, Bruce Mathewson, Francisco Socal, Durgesh Srivastava, Dong Wei

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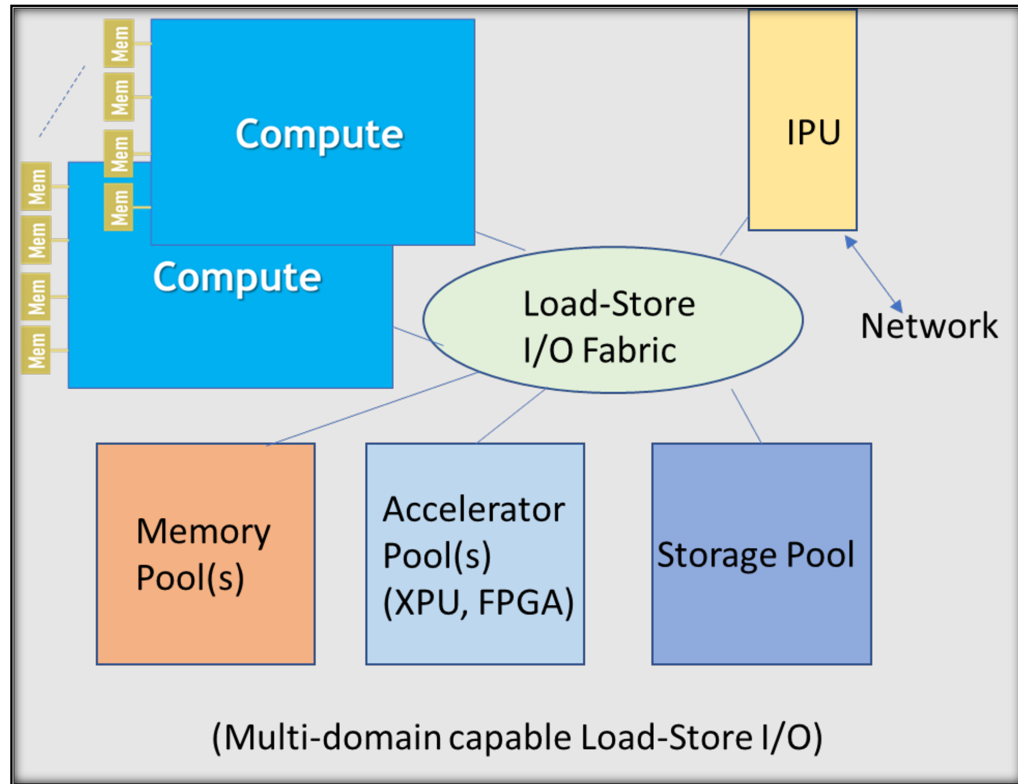
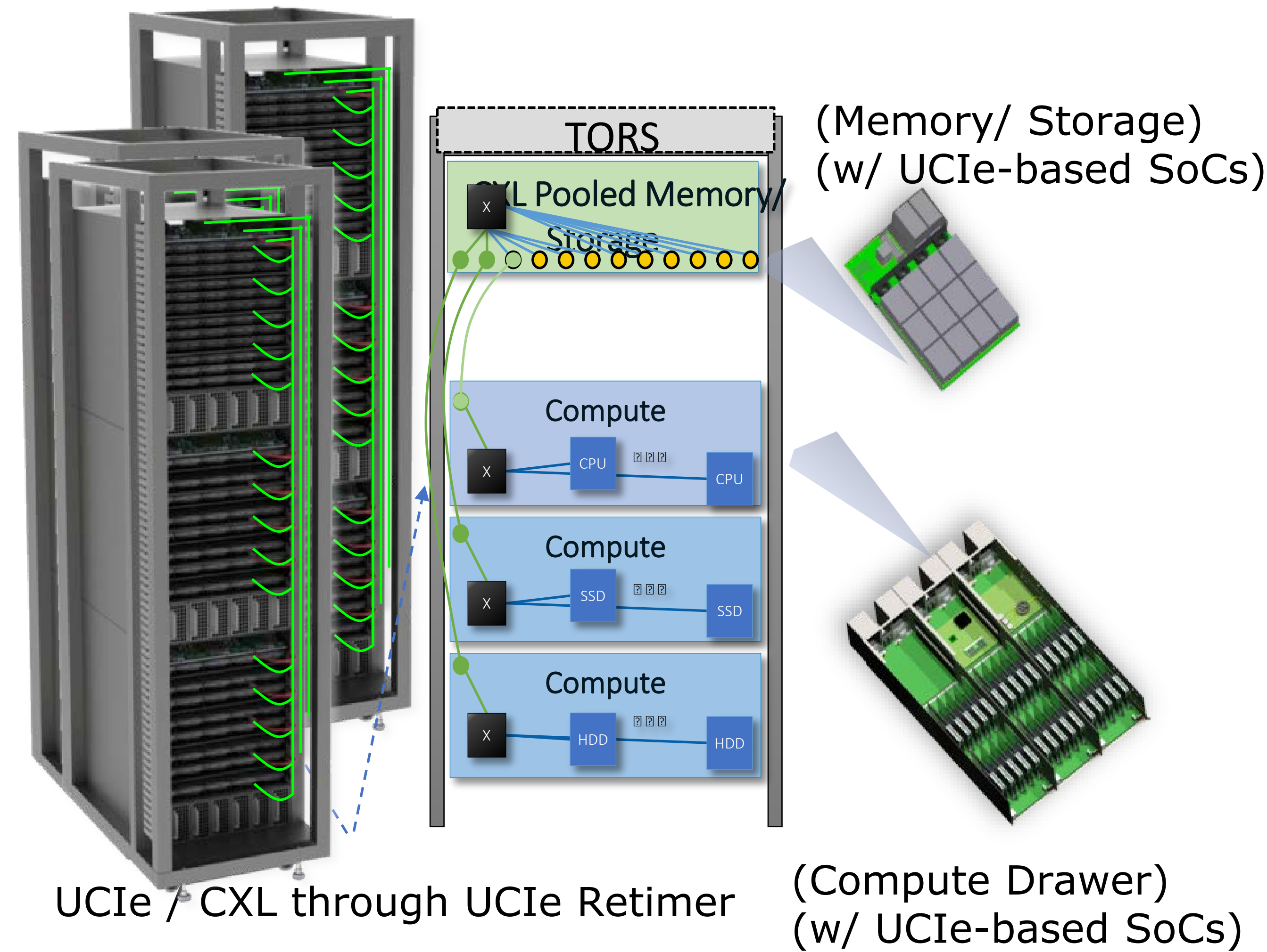
# UCIe Usage: Off-package Connectivity w/Retimers



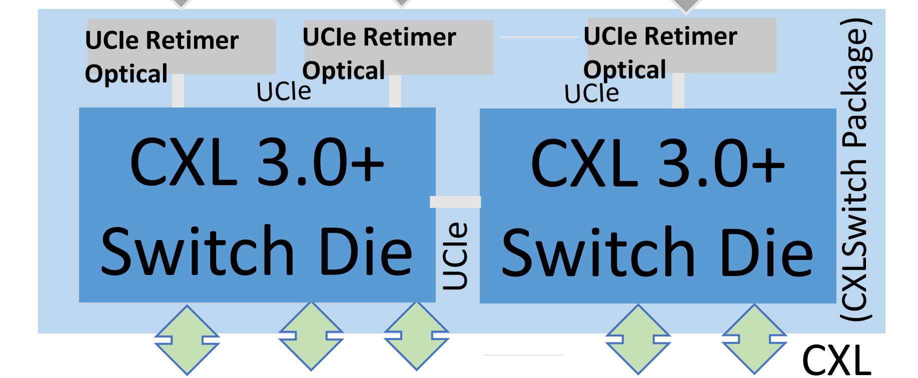

(Use Case: Load-Store I/O (CXL) as the fabric across the Pod providing low-latency and high bandwidth resource pooling/ sharing as well as message passing)

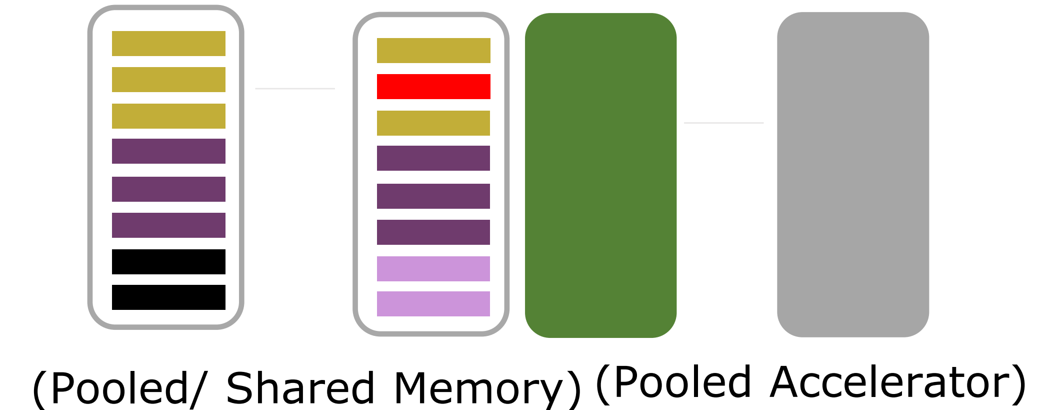



UCIe / CXL through UCIe Retimer

Provision to extend off-package with UCIe Retimers connecting to other media (e.g., optics)

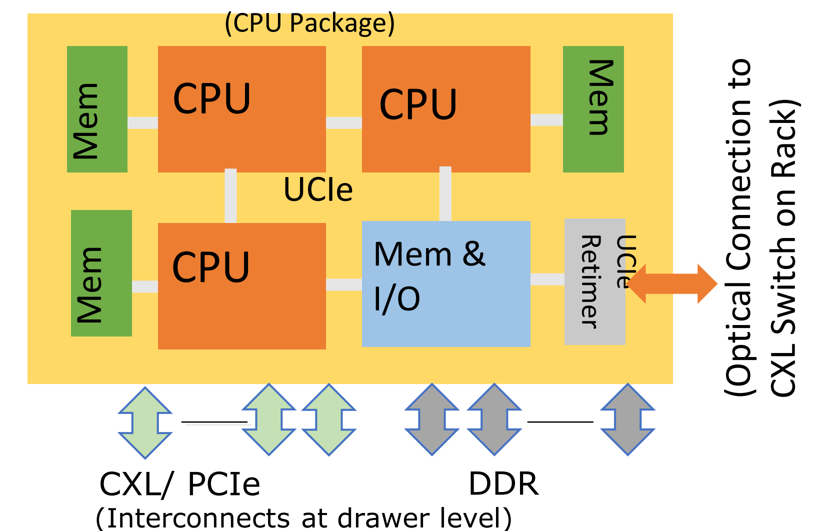
(Optical connections: Intra-Rack and Pod)




(Pooled/ Shared Memory) (Pooled Accelerator)

(Switch dies connected through UCIe PHY + Adapter Running a proprietary switch internal protocol)




(Another example can be multi-terabit networking switches Constructed from UCIe-based co-packaged optics and partitionable networking switch dies connected through UCIe on package

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# UCIe 1.0/ 1.1: Characteristics and Key Metrics

| CHARACTERISTICS | STANDARD PACKAGE | ADVANCED PACKAGE | COMMENTS |
|---|---|---|---|
| Data Rate (GT/s) | 4, 8, 12, 16, 24, 32 | | Lower speeds must be supported -interop (e.g., 4, 8, 12 for 12G device) |
| Width (each cluster) | 16 | 64 | Width degradation in Standard, spare lanes in Advanced |
| Bump Pitch (um) | 100 – 130 | 25 - 55 | Interoperate across bump pitches in each package type across nodes |
| Channel Reach (mm) | <= 25 | <=2 | |

| KPIs / TARGET FOR KEY METRICS | STANDARD PACKAGE | ADVANCED PACKAGE | COMMENTS |
|---|---|---|---|
| B/W Shoreline (GB/s/mm) | 28 – 224 | 165 – 1317 | Conservatively estimated: AP: 45u; Standard: 110u; Proportionate to data rate (4G – 32G) |
| B/W Density (GB/s/$mm^2$) | 22-125 | 188-1350 | |
| Power Efficiency target (pJ/b) | 0.5 | 0.25 | |
| Low-power entry/exit latency | 0.5ns <=16G, 0.5-1ns >=24G | | Power savings estimated at >= 85% |
| Latency (Tx + Rx) | < 2ns | | Includes D2D Adapter and PHY (FDI to bump and back) |
| Reliability (FIT) | 0 < FIT (Failure In Time) << 1 | | FIT: #failures in a billion hours (expecting ~1E-10) w/ UCIe Flit Mode |

UCIe 1.0/1.1 delivers the best KPIs while meeting the projected needs for the next 5-6 years across the compute continuum.

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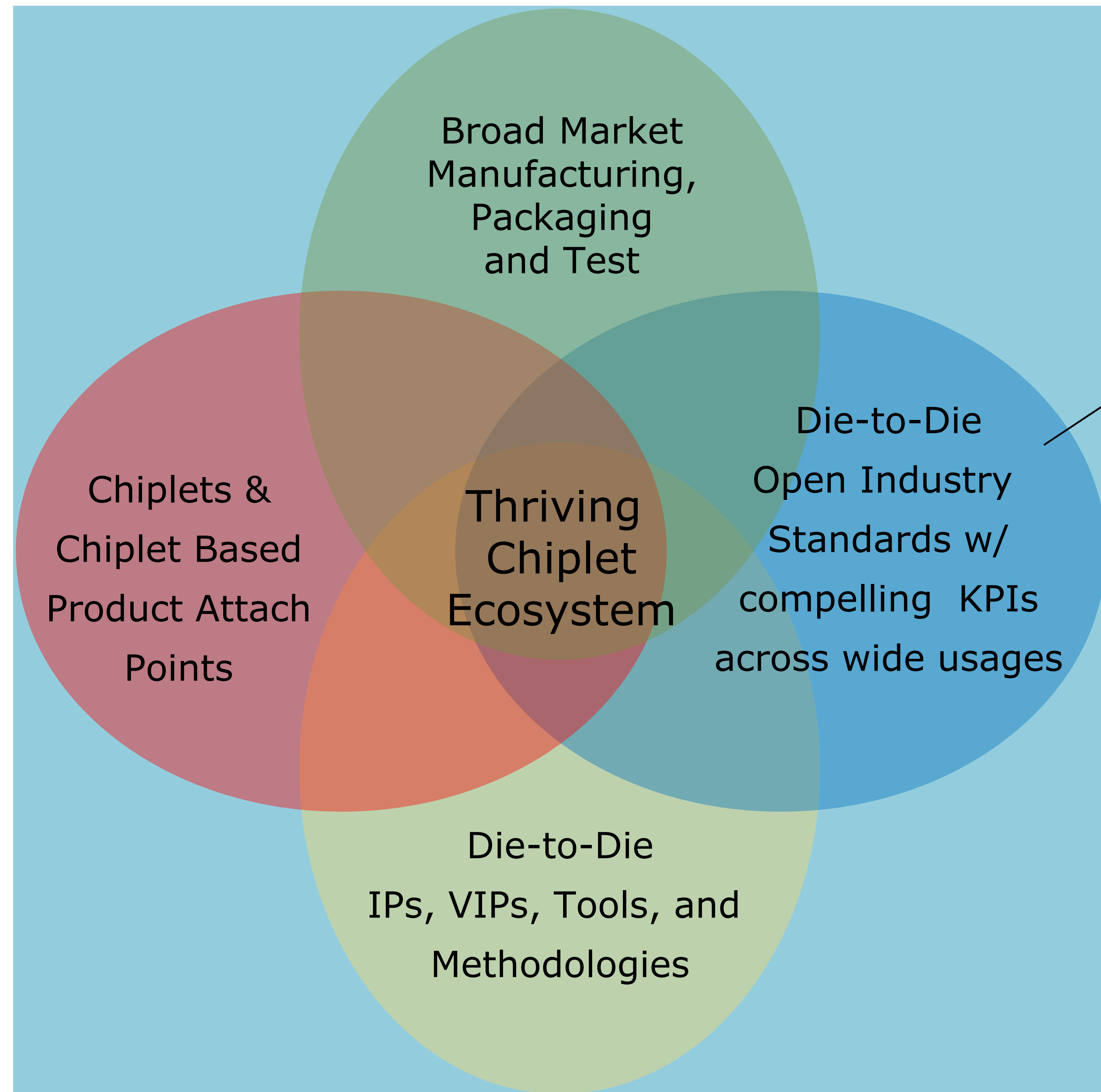
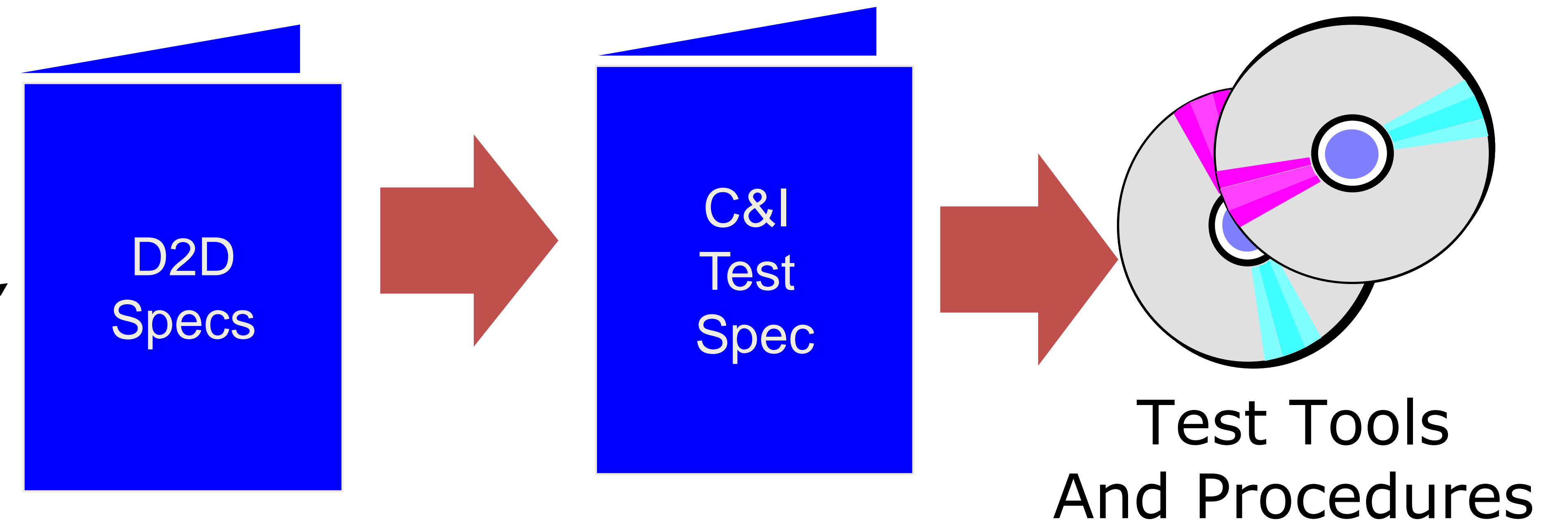
# Ingredients for a Broad Inter-operable Chiplet Ecosystem




Test Tools And Procedures

Well-defined Specs

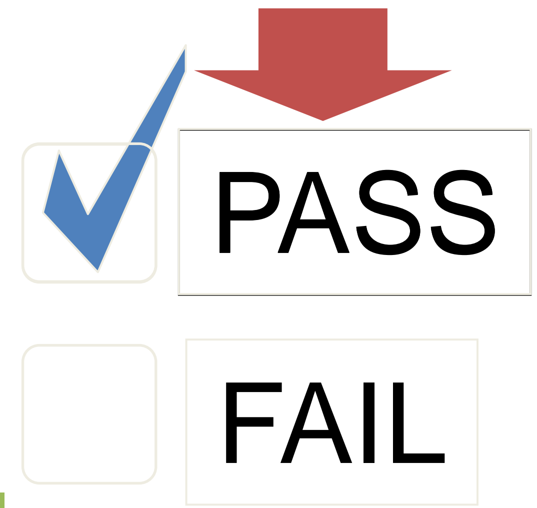
(Electrical, Logical, Protocol (e.g., PCIe/ CXL) Software, Form-Factor, Management)

Test criteria based on Specs

(Test Definitions, Pass/Fail Criteria: Electrical, Logical, Protocol, Software)

Test H/W & S/W *Validates* Test criteria

- Compliance
- Interoperability




**Predictable path to design compliance with UCIe**

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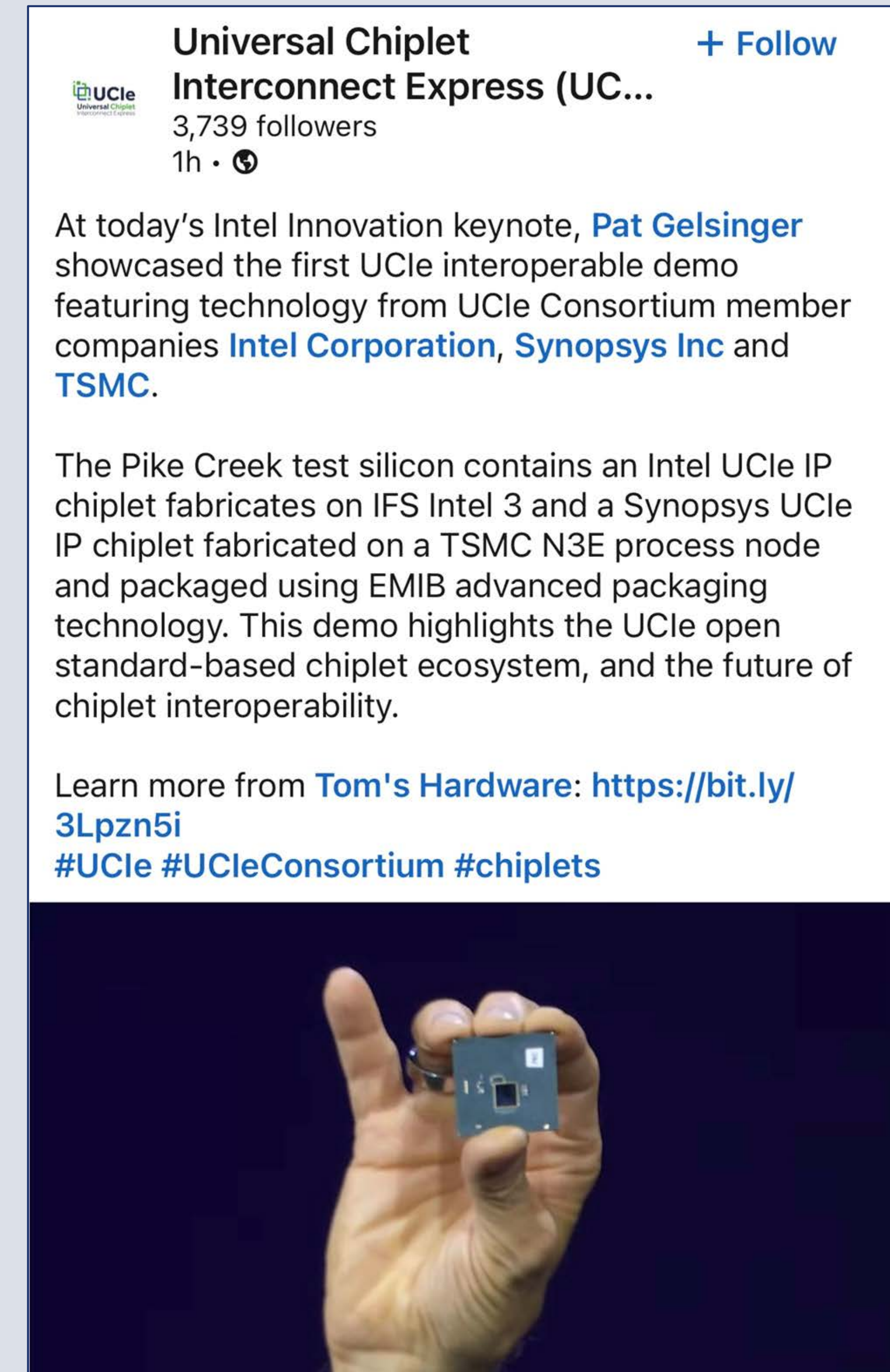
# The First UCIe Silicon Interoperability: Intel silicon on Intel Process with Synopsys silicon on TSMC process

**Sept 19, 2023**

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# Summary

- **UCIe Consortium continues to evolve the UCIe Technology in a backward-compatible manner comprehending new usage models, additional cost optimization, and a robust compliance mechanism**

- **UCIe is an open industry standard that establishes an open chiplet ecosystem and ubiquitous interconnect at the package level.**
  - Tremendous support across the industry with several companies announcing IP/VIP availability
  - Evolving as the interconnect of SoCs the same way PCIe and CXL did at the board level
  - UCIe 1.1 Specification is available to the public https://www.uciexpress.org/specification

- UCIe Consortium welcomes interested companies and institutions to join the organization at the **Contributor or Adopter level**.

- 6 **Technical Working Groups** (Electrical, Protocol, Form Factor/Compliance, Manageability / Security, Systems and Software, Automotive) and **Marketing Working Group** driving the technology forward
  - Plenty of innovations happening in the consortium

- **Join us if you have not done so! Learn more by visiting** www.UCIexpress.org

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# Q&A

*Please share your questions in the Question Box*

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# Thank You

www.UCIexpress.org

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