Introducing the UCIe™ 3.0 Specification: Continued Innovations in the Open Chiplet Ecosystem

UCIe Universal Chiplet Interconnect Express

Meet the Presenter

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UCIe Consortium Chairman

UCIe™ Universal Chiplet Interconnect Express

Disclaimer

The information in this presentation may refer to a specification still in the development process. This presentation may reflect the current thinking of various UCIe™ workgroups, but all material is subject to change as specifications are developed.

Agenda

- Introducing UCIe
- Overview of UCIe 1.0/1.1/2.0
- UCIe 3.0 Enhancements for Planar (UCIe-A, UCIe-S):
  - Improving bandwidth density: 48 GT/s and 64 GT/s support
  - New Usage: Support for Continuous Transmission Protocols
  - Operational Power Savings: Run-time TX recalibration
  - Idle Power Savings: L2 Optimization
  - Manageability enhancements for seamless Interoperability
    - Firmware Download
    - Priority Packets in Sideband
    - Extending sideband reach for star topology
    - Open drain pin support
    - Fast throttle/ Shutdown
- Key Metrics with UCIe 3.0
- Future Directions and Conclusions

UCIe™ Universal Chiplet Interconnect Express

Universal Chiplet Interconnect Express™ (UCIe™)
An Open Standard for Chiplet Development

- UCIe Guiding Principles
  - Open chiplet ecosystem
  - Backward-compatible evolution to ensure investment protection
  - Optimized power, performance, and cost metrics applicable across the entire compute continuum
  - Continuously innovate to meet the needs of the evolving ecosystem

Leveraging decades of experience driving successful industry standards at the board level: PCIe, CXL, USB, etc.

High-bandwidth, Low-latency, Power-efficient, Cost-effective Interconnects for
AI, HPC, Cloud, Edge, Enterprise, 5G, Automotive, Handhelds

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Board Members

Leaders in semiconductors, packaging, IP suppliers, foundries, and cloud service providers are joining together to drive the open chiplet ecosystem.

JOIN US!

Alibaba Cloud
AMD
arm
ASE GROUP
Google Cloud
intel.
Meta
Microsoft
NVIDIA
Qualcomm
SAMSUNG
tsmc

140+ Member Companies…and growing!

UCIe™
Universal Chiplet Interconnect Express

UCIe Consortium is Open for Membership

- UCIe Consortium welcomes interested companies and institutions to join the organization at the **Contributor and Adopter level**.

- UCIe was founded in March 2022, incorporated in June 2022. Two levels of memberships: Contributor and Adopter

- **Contributor Membership**
  - Access the Final Specifications (ex: 1.0, 1.1, 2.0, etc.)
  - Implement with the IP protections as outlined in the Agreements
  - Right to attend Corporation trade shows or other industry events as determined by the Board
  - Participate in the technical working groups
  - Influence the direction of the technology
  - Access the intermediate (dot level) specifications
  - Election to get to the Promoter Class/ Board every year when the term of half the board completes

- **Adopter Membership**
  - Access the Final Specifications (ex: 1.0, 1.1, 2.0, etc.), but not intermediate level specifications
  - Implement with the IP protections as outlined in the Agreements
  - Right to attend Corporation trade shows or other industry events as determined by the Board

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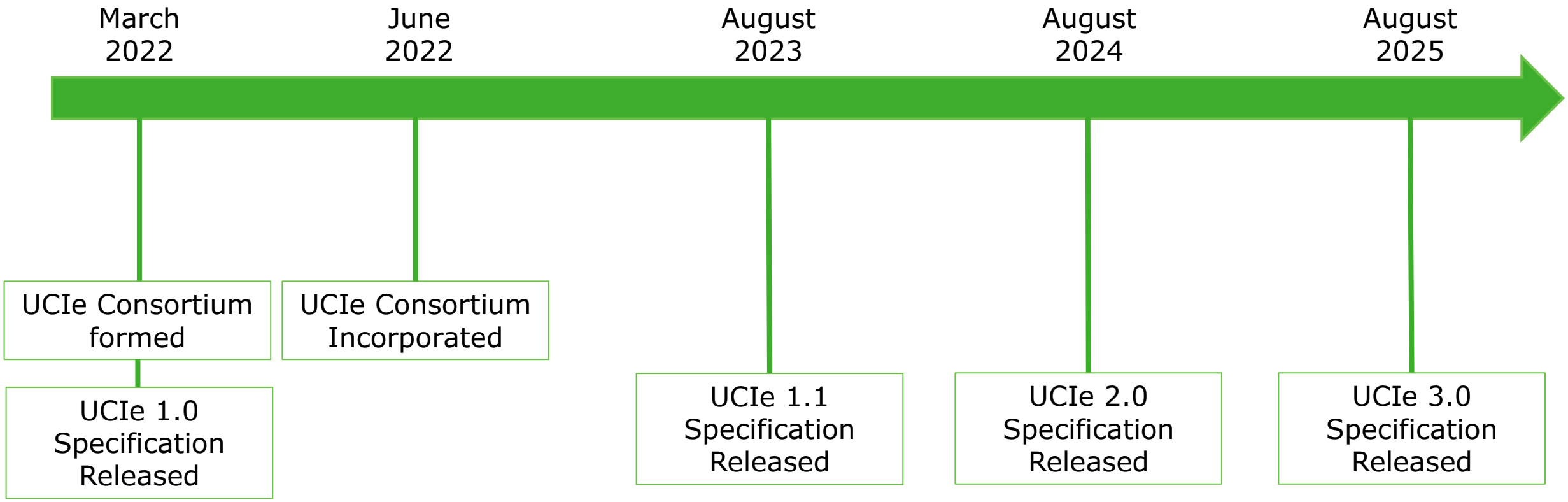
Member-Driven Evolution



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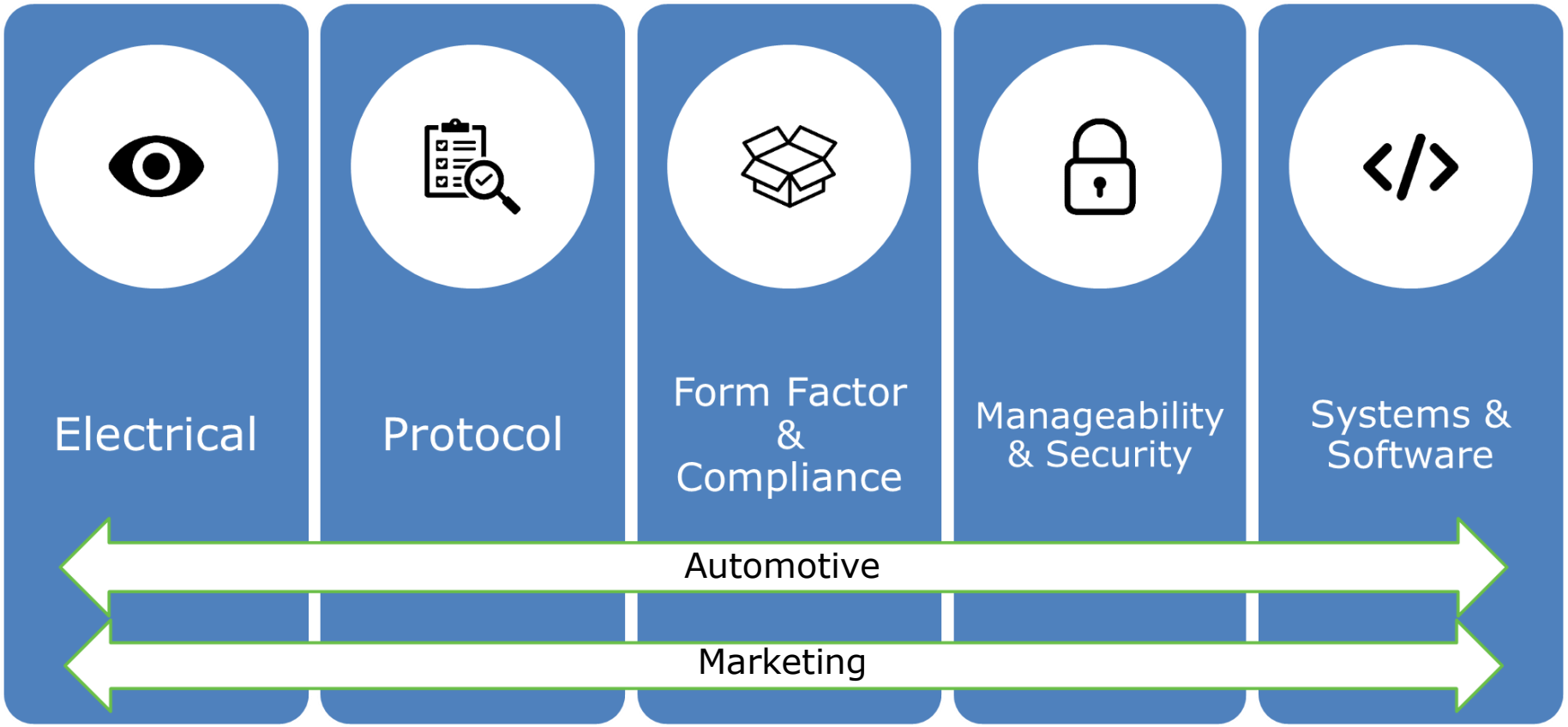
UCIe Consortium Working Groups

- Working Groups are identifying and addressing the demands of a complete, full-stack solution for strengthening the open standards-based ecosystem.



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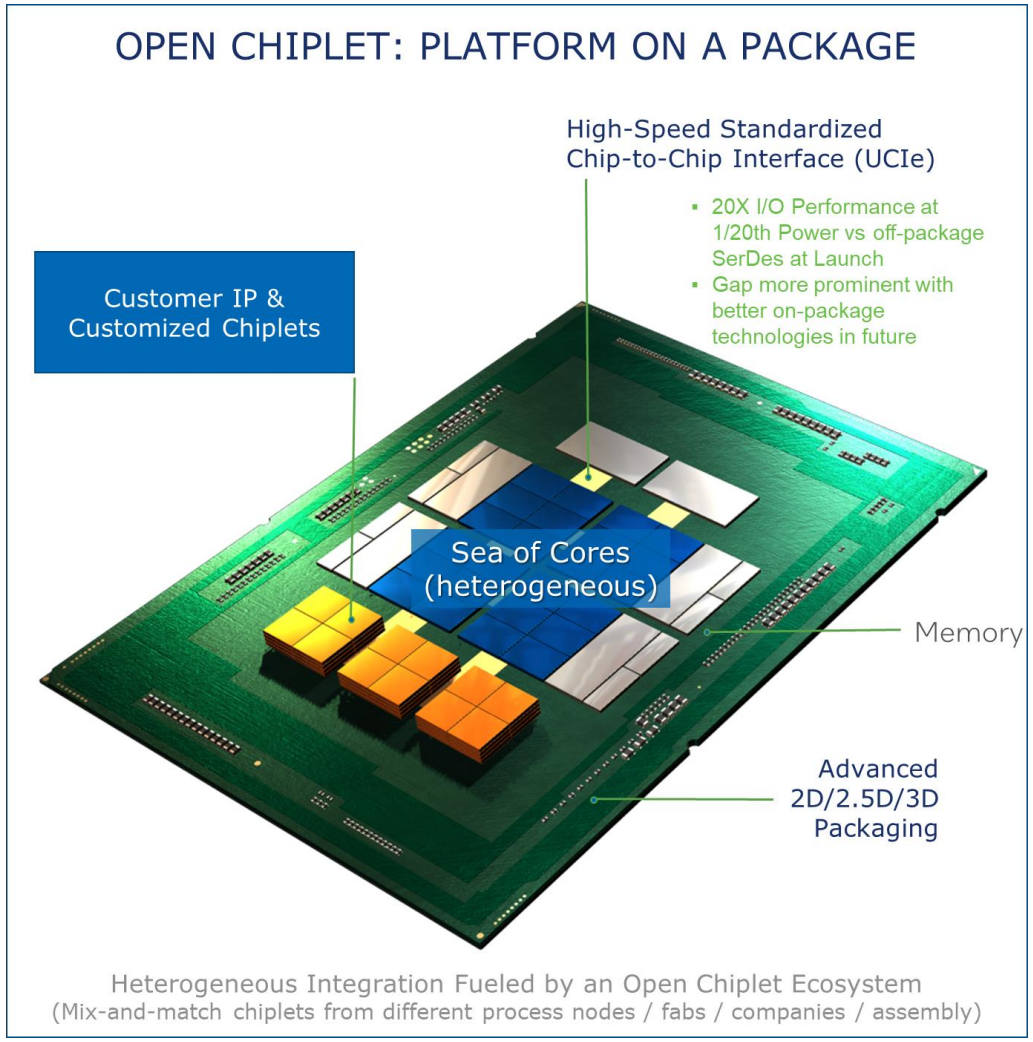
Motivation for UCIe



- Overcome reticle limits – SoC is now at package level
- Reduces time-to-solution (e.g., enables die reuse)
- Lowers portfolio cost (product & project)
  - Optimal process
  - Smaller dies => better yield
  - Reduces IP porting costs
  - Lowers product SKU cost
- Bespoke solution
  - Mix-and-match with a standard interface
- Scales innovation (Mfg. process locked IPs)

UCIe driving Industry alignment! Package is the new platform!

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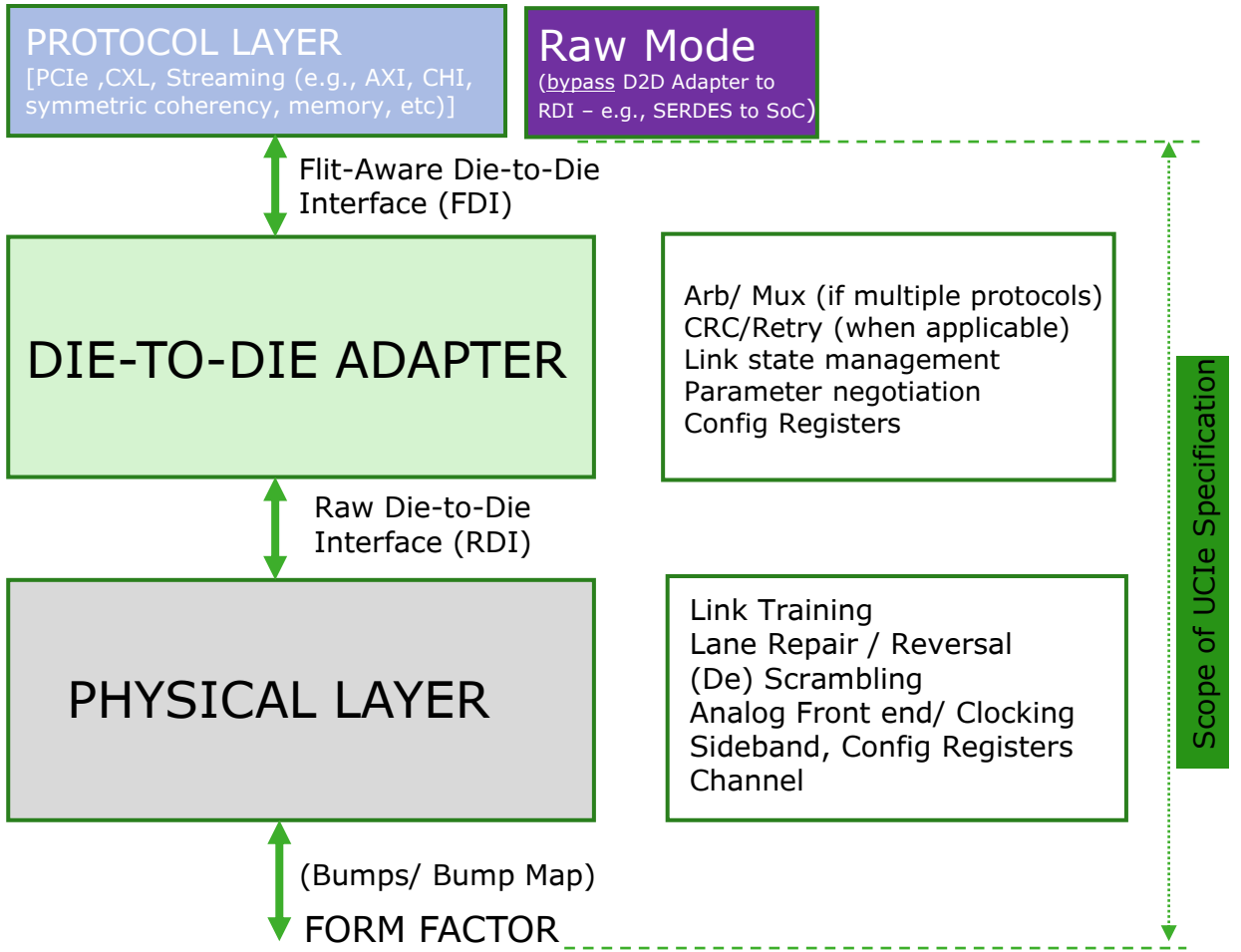
UCIe 1.0 and 1.1 Specifications for Planar Interconnects

- **Layered Approach - industry-leading KPIs**
- **Planar: UCIe-S (2D) and UCIe-A (2.5D)**
- **Physical Layer:** Die-to-Die I/O
- **Die to Die Adapter:**
  - Reliable delivery, Multi-protocol support
- **Protocol**:
  - **CXL®/PCIe® for volume attach, plug-n-play**
  - SoC construction issues are addressed w/ CXL/PCIe
  - Usages: I/O attach, Memory, Accelerator
  - **Streaming for other protocols**
    - Scale-up (e.g., CPU/ GP-GPU/Switch from smaller dies)
- **Well defined specification**
  - Configuration register for discovery and run-time
  - Form-factor and Management
  - Compliance for interoperability
  - Plug-and-play IPs with RDI/ FDI interface



More Information at: www.uciexpress.org (whitepapers and webinars):

1. White Papers: https://www.uciexpress.org/ucie-resources : "UCIe: Building an open chiplet ecosystem", and "UCIe 1.1.."
2. Webinars: https://www.uciexpress.org/webinars : "Introduction to UCIe" (Feb 21, 2023)and "UCIe 1.1 Specification" (Oct 12, 2023)

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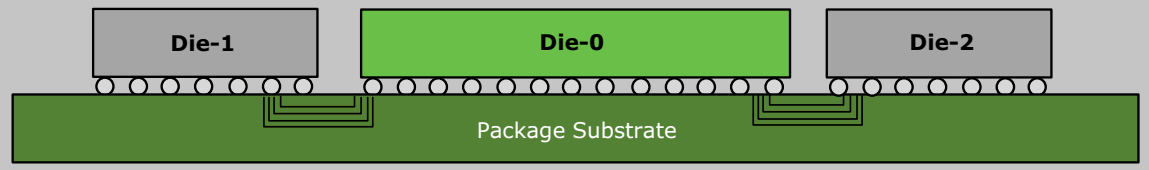
UCIe 1.0/1.1: Supports Standard and Advanced Packages

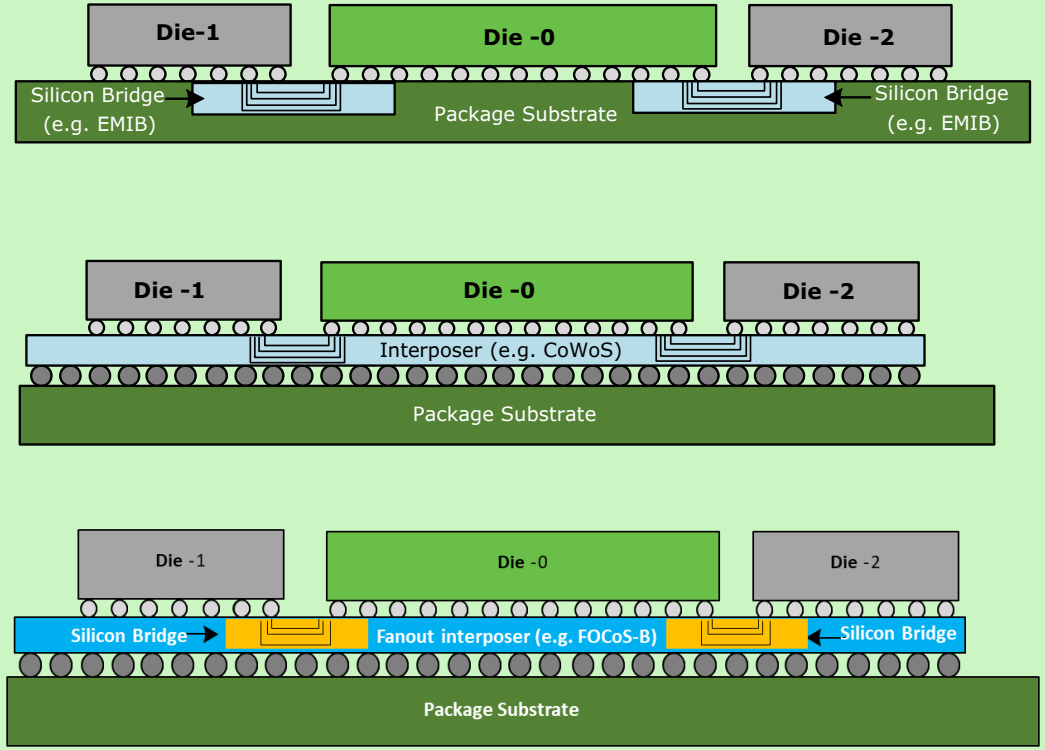


(Standard Package)

Standard Package: 2D – cost effective, longer distance

Advanced Package: 2.5D – power-efficient, high bandwidth density

Dies can be manufactured anywhere and assembled anywhere – can mix 2D and 2.5D in same package: Flexibility for SoC designer



(Multiple Advanced Package Options)

More Information at: https://www.uciexpress.org/webinars : "UCIe Packaging Technologies" (June 15, 2023) and "Exploring the Advancement of Chiplet Technology and the Ecosystem" (April 17, 2024)

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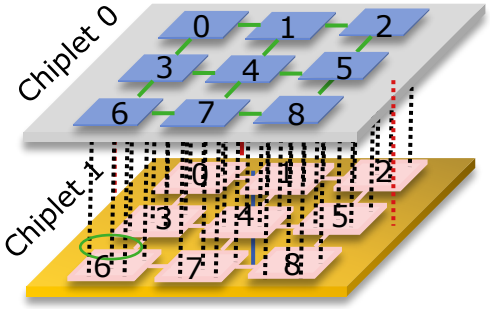
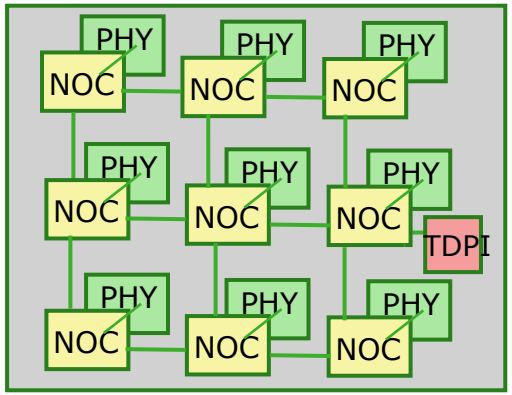
UCIe 2.0: Vertical Chiplets with UCIe-3D

- 3D deployed in commercial offerings (Memory, CPU)
  - Hybrid bonding (HB) looks promising – bump pitch: 9u -> <1u
  - Standardize for constrained interop (e.g., bump pitch match)
- High bandwidth density
  - 3D => areal connectivity (vs shore-line in 2D/ 2.x D)
  - Number of wires increases inversely as the square of bump pitch
  - Must ensure we continue to be bump-limited
- Low power
  - Reduced interconnect distance (~0) between dies, electrical parasitics
- Simple circuits and lower frequency are essential
  - No D2D adapter, SoC frequency, cluster-level repair
- Better power, bandwidth, and latency than UCIe 2.5D





UCIe-3D delivers power-efficient performance comparable/ better than large monolithic die

More Information at: www.uciexpress.org (whitepapers and webinars):

1. White Papers: https://www.uciexpress.org/ucie-resources : "UCIe 2.0 Specification: …"
2. Webinars: https://www.uciexpress.org/webinars : "Introduction the UCIe 2.0…" (Sept 19, 2024)and "A deep-dive..UCIe-3D" (Dec 4, 2024)

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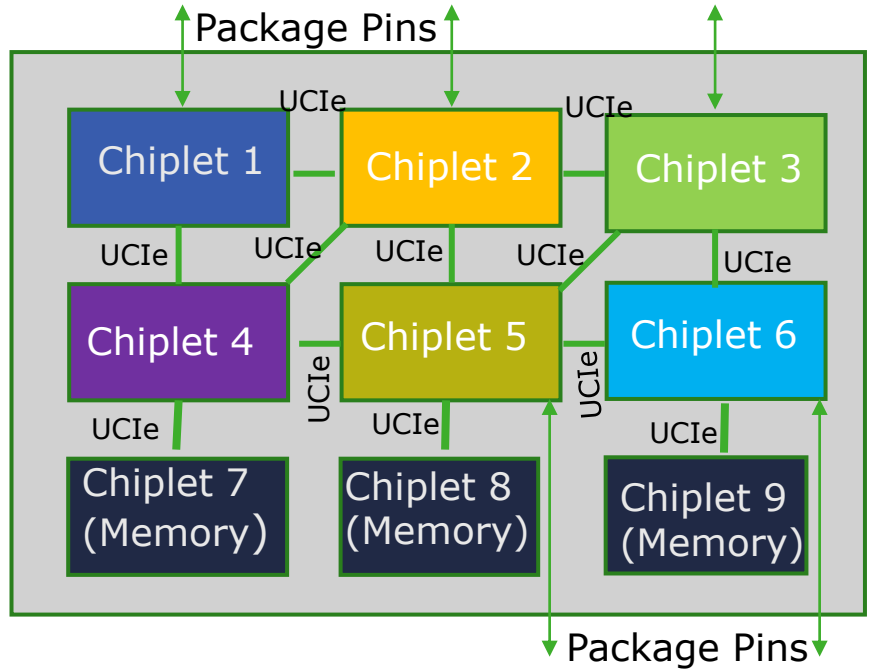
UCIe 2.0: Testability, Manageability, Debug

- Test: Die / Sort, Package / Bond
  - Micro-bumps can not be probed
  - Use other bumps (e.g. JTAG, UCIe-S)
- Repair: assembly & in field (UCIe)
- Debug and Manageability w/ security
  - lab, field – no analyzer/ scope
- Some chiplets may not have access to package pins
  - Use UCIe-S (dedicated or shared, sideband only or mainband) to access remote chiplets from chiplets with package pins
- Definition of management fabric comprising of ports, elements, director communicating through packets and software infrastructure leveraging industry standards like MCTP supporting a wide range of bandwidth demands

A common UCIe test/debug/mgmt infrastructure that can work through the entire lifecycle with UCIe 2.0



Interface	Bandwidth
UCIe-S x16	512 Gb/s/dir main @ 32G (800 Mb/s/dir sideband)
PCIe6.0 x16	1024 Gb/s/dir
USB 4.0	80 Gb/s/dir
JTAG /1838	5-100+ Mb/s/dir
I3C	33 Mb/s/dir

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Doubling Data Rates for UCIe-A and UCIe-S

- **Motivation:** Continued demand for higher linear bandwidth density for SoCs used applications such as AI, HPC, etc. with shore-line constraints
- **Solution:** Increase the data rate from maximum 32 GT/s to 48 and 64 GT/s
- **UCIe's Approach**:
  - Full backwards compatibility – same sideband, valid, track, data, training, etc.
  - Signaling: NRZ Uni-directional
  - Clocking: Quarter rate for 48/64 GT/s; free running
  - BER: 10-15 for 48 GT/s and 10-12 for 64 GT/s
  - Termination: RX Termination required for both UCIe-S and UCIe-A
  - Enhanced Equalization: 3-tap TX FFE (1-pre + 1-post); 1st order (passive) RX CTLE : can possibly be combined with T-coil network; Optional 1-tap RX DFE
  - B/W Density target: 1.7-2x linear, 1.3-1.6x areal.
  - Power Target: 0.5-0.75pJ/b
    - Break down: ~ 40% TX, 40% RX, 20% common circuits.
- **Result:** Linear B/W Density increases 1.65x/2x for UCIe-S/UCIe-A with similar power efficiency

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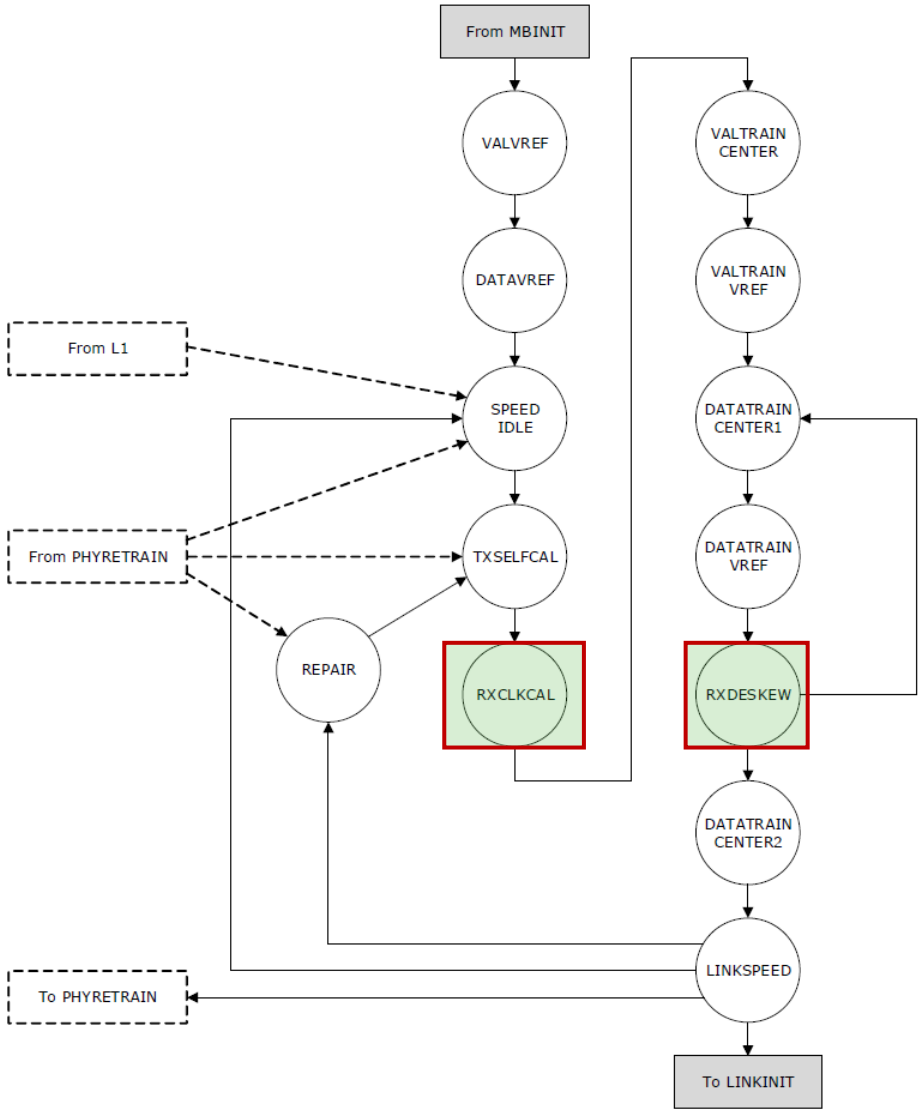
Clocking

- **Quarter rate** and **free running clock** only for 48 and 64 GT/s
- Valid Framing and Fast Idle Entry/Exit through Valid Gating remain the same

Forward Clock Frequency and Phase:

Data Rate (GT/s)	Clock freq. (fCK) (GHz)	Phase-1	Phase-2	Deskew (Req/Opt)
64	16	45	135	Required
48	12	45	135	Required
32	16	90	270	Required
	8	45	135	Required
24	12	90	270	Required
	6	45	135	Required
16	8	90	270	Required
12	6	90	270	Required
8	4	90	270	Optional
4	2	90	270	Optional

Training and Equalization at 48/64 GT/s



- I/Q training done in RXCLKCAL phase
- EQ adjustments done in RXDESKEW
  - TX Preset selection (of 6) is accomplished in RXDESKEW phase
  - Pick best Preset based on RX Eye Margin
  - Can go back to DATATRAIN CENTER1 if more training time is needed

Preset Table:

	C(-1)	C(0)	C(+1)	Accuracy
P0	0	1	0	
P1	-0.05	0.95	0	+/- 0.025
P2	0	0.9	-0.1	+/- 0.025
P3	-0.05	0.85	-0.1	+/- 0.025
P4	0	0.8	-0.2	+/- 0.025
P5	-0.05	0.75	-0.2	+/- 0.025

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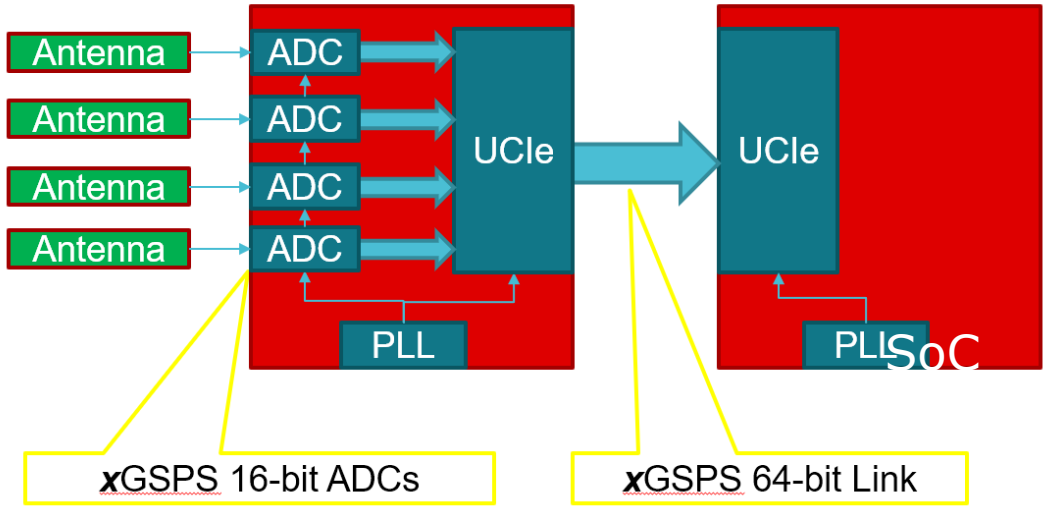
New Usage: Support for Continuous Transmission Protocols

- **New Usage:** Continuous transmission applications (e.g., DSP) like a separate ADC chip connected to SoC
  - Leading DSP companies wanted to use UCIe standard
  - Run link at same data rate as data generation/ consumption
  - No need for separate PLLs
  - Avoids introducing additional frequency noise in sensitive analog circuits
  - Need periodic synchronization markers, parity
- **UCIe's Approach:**
  - Use existing raw mode with enhancements to the internal RDI / FDI interface
  - Reuse the UCIe Retimer encodings in Valid to send periodic synchronization markers and parity (full use of all data lanes which is desired)
    - E.g., 0000_1111b in valid indicates valid framing plus a synchronizer marker (1111_1111b is valid framing but no synchronizer marker) – 1 bit per 8 UI from the retimer credit release encoding
  - Support range of frequencies



Link Speed Setting	Min Adjusted Operating Speed	Max Adjusted Operating Speed
4 GT/s	2 GT/s	4 GT/s
8 GT/s	4 GT/s	8 GT/s
12 GT/s	8 GT/s	12 GT/s
16 GT/s	12 GT/s	16 GT/s
24 GT/s	16 GT/s	24 GT/s
32 GT/s	24 GT/s	32 GT/s
48 GT/s	32 GT/s	48 GT/s
64 GT/s	48 GT/s	64 GT/s

Continuous Mode Transmission

- System designer controls the data rate by varying the REFCLK provided to the PLLs in the UCIe IP (see table for range)
  - IP will work since the change is with Refclk and it is within the interoperability range
- Compliance only performed for the UCIe data rates supported by the UCIe IP (i.e. Link Speed Setting in the table below)

Link Speed Setting	Min Adjusted Operating Speed	Max Adjusted Operating Speed
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8 GT/s	4 GT/s	8 GT/s
12 GT/s	8 GT/s	12 GT/s
16 GT/s	12 GT/s	16 GT/s
24 GT/s	16 GT/s	24 GT/s
32 GT/s	24 GT/s	32 GT/s
48 GT/s	32 GT/s	48 GT/s
64 GT/s	48 GT/s	64 GT/s

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Runtime Recalibration Enhancement

- Power savings feature for UCIe Physical Layer
- Permits TX adjustment of clock to data skew during runtime recalibration of the Link (previously was only available on the Rx side)
- Saves power because Tx has wider adjustment range already during Link Initialization flows, and can repurpose that during runtime recalibration

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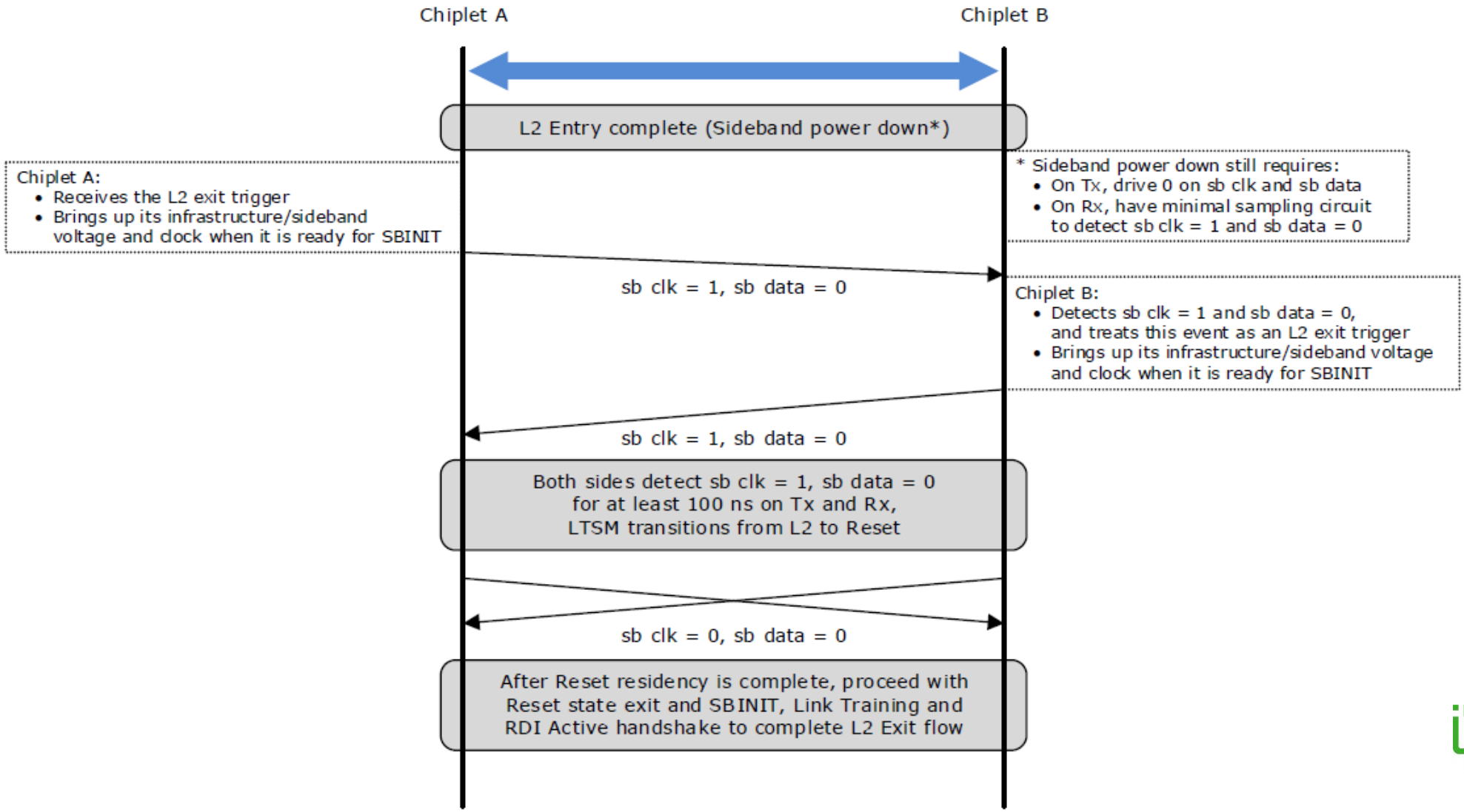
L2 Exit Handshake

- **Motivation:** Deeper power savings by turning off power and clock to sideband infrastructure in L2, the deep power saving state
  - Main band is already off
- **What is needed:** A mechanism to wake up the sideband infrastructure on L2 exit and initialize it before sideband packets can be exchanged
- **Approach:**
  - Use the existing sideband clock and data pins (no new wires) to indicate L2 exit using DC signal levels (see flow on next slide)
  - A small amount of logic is active while the rest of sideband is powered off/ clock gated to detect exit from L2 and wake up the rest of sideband
  - Rules are provided such that the exit can be symmetric or one sided

L2 Optimization Flow



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Early Firmware Download: Motivation

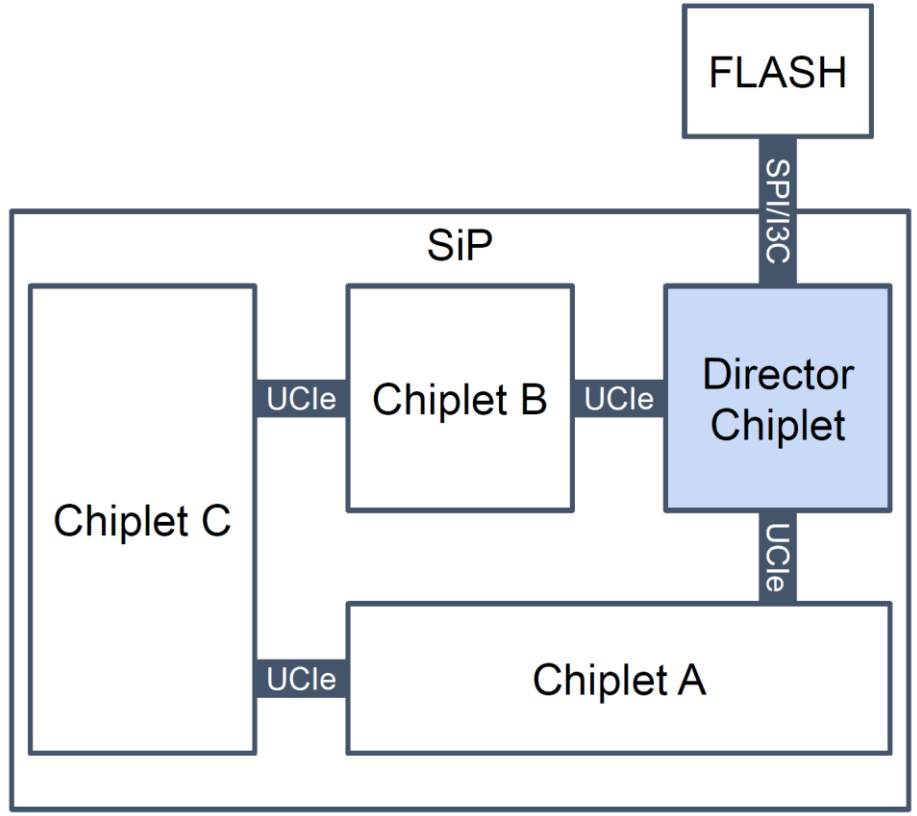
- A chiplet might need firmware to function properly. Examples:
  - For interface and internal structures bring up (SERDES, memory)
  - For Management features support
- We want to avoid:
  - Every chiplet having its own external flash or firmware loading mechanisms
  - Chiplet to implement MCTP / PLDM firmware download in immutable firmware
- Our solution allows to download first mutable firmware:
  - Simple registers mechanism, can work using UCIe side band
  - Can be implemented with a simple hardware FSM
  - Can support secure requirement (staging)

Flow Overview

- Director Chiplet
  - Obtains Firmware (e.g., by loading FW from an external Flash)
  - Initialize side-band management network
  - Download first mutable firmware to chiplets
- Chiplet waits for director to download firmware

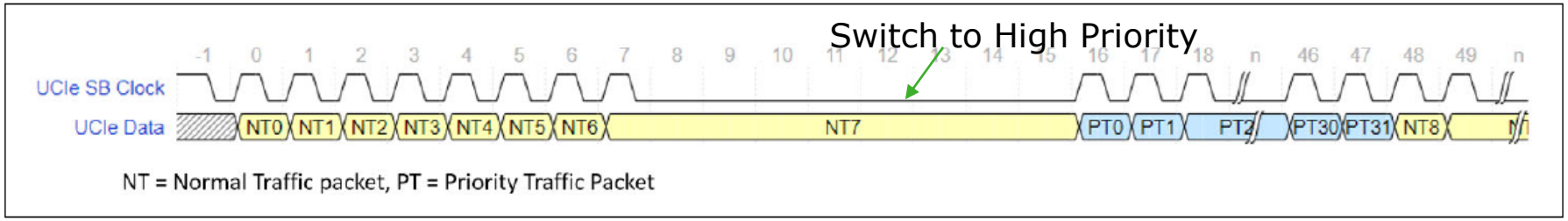
  ⇒ Chiplet boot with first mutable firmware

  ⇒ Chiplet can request further firmware update
  - Through side-band
  - Through main-band
  - Using MCTP / PLDM / …
- Data structures like circular buffer are also defined for interoperability between chiplets



Priority Sideband Packets

- Motivation: Several events need high priority notification over others
  - Example: Power down, Power wake up, low-latency telemetry data, power supply switch to redundant supply – needs 1-10 us latency. Do not want these to be stuck behind say a FW download/ debug dump
- Approach: Create a mechanism to interrupt sideband packets ("normal traffic") at an 8UI interval to insert the priority vector ("priority traffic") that is to be transported to the remote Link partner
- Mechanism:
  - A trigger from the transmitter to indicate it is switching to "priority traffic" from "normal traffic"
    - This trigger is in the form of the clock remaining 0b for 8UI before beginning the priority transfer.
    - The receiver detects this (implementation specific means), and it expects a priority vector next.
  - The priority vector is sent from transmitter to receiver – total 32UI, with 23 bits for the vector, 5b opcode, 3 reserved bits and 1 bit even parity.
  - After this 32UI has completed, the packet from "normal traffic" is resumed or another priority packet can be sent (based on opcode) without any gaps in clock
  - Max time to transfer priority packet: 8UI (boundary) + 8UI (switch) + 32 UI (transfer) = 48 UI = 60 ns



Extended Reach Sideband (UCIe-S Only)

- Permit 100mm sideband channel to minimize hops/daisy chaining in SiP (enables practical usage of Star topology in SiP with sideband)
  - Connect the Director Chiplet directly to each chiplet for better manageability and security using a UCIe-S SB only link
- UCIe 2.0 Specification: Sideband like main-band reach specified at 25 mm, even for sideband-only link
- Given that the operating frequency is 800 MHz, we can easily extend that reach to 100mm for sideband
- Details: Provide appropriate guidelines for the extended reach
  - Vih = 70% of VCCAON, Vil = 30% of VCCAON
  - At Longer Channel Lengths, Slope is not a meaningful measurement. Waveforms take a long time to reach 0.8*VCCAON, and sometimes do not reach 80% of VCCAON. So, Txron is a more meaningful measurement for measuring Eye Height and Eye Width.
  - For longer reach, Driver Ron needs to be limited to 60 Ohm worst case (including worst case errors and supply variations)

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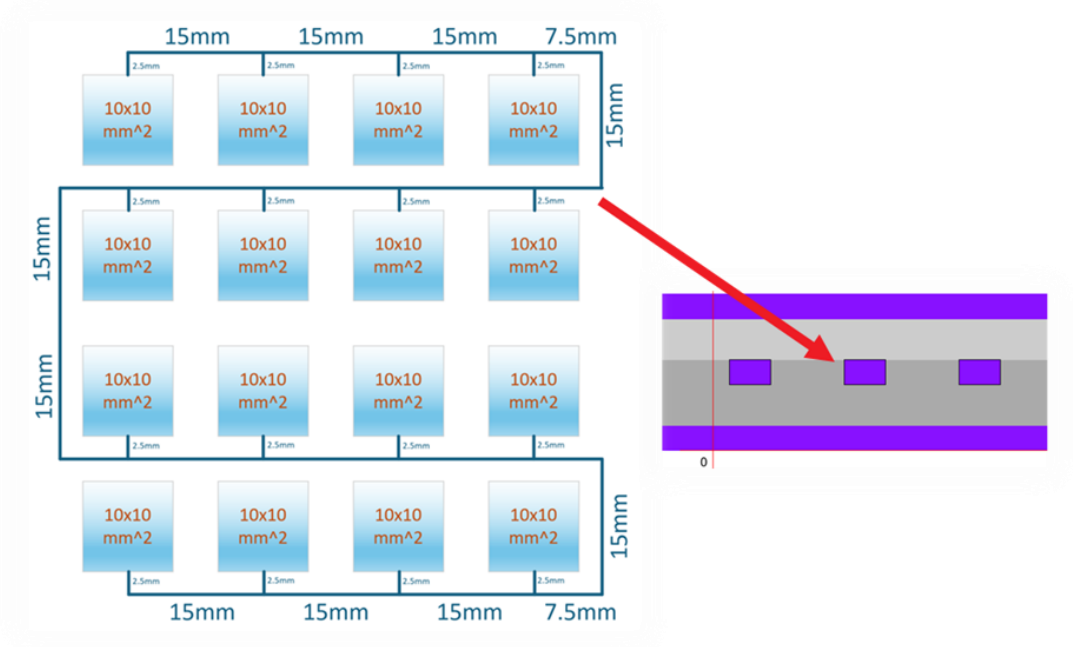
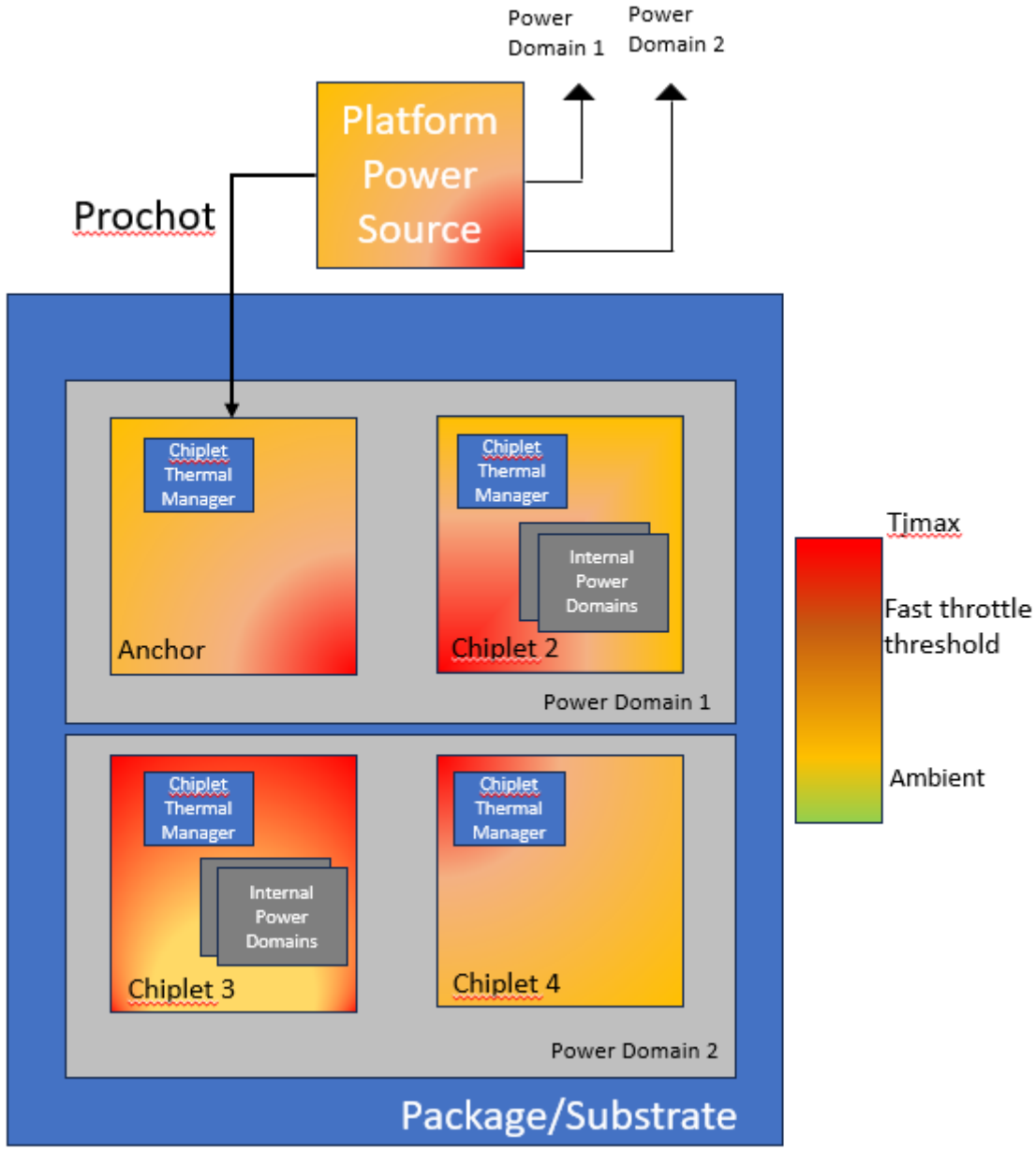
Open Drain Pins

- Motivation: Critical events like emergency shutdown or fast throttle need SiP wide simultaneous broadcast to all chiplets
- Open Drain pins enable low latency, bi-directional events. They are used for certain UCIe specified events, such as Emergency Shutdown and Fast Throttle, as well as vendor-defined events.
- The Open Drain pin is intended for package-level routing and need not be on the same shoreline as the UCIe macro. All specifications are based on package-level routing. Same pins irrespective of the number of UCIe-S/-A/-3D links between any two chiplets on the SiP

Worst case package route for open-drain signal



Fast Throttle and Emergency Shutdown



Problem Statement/ Motivation

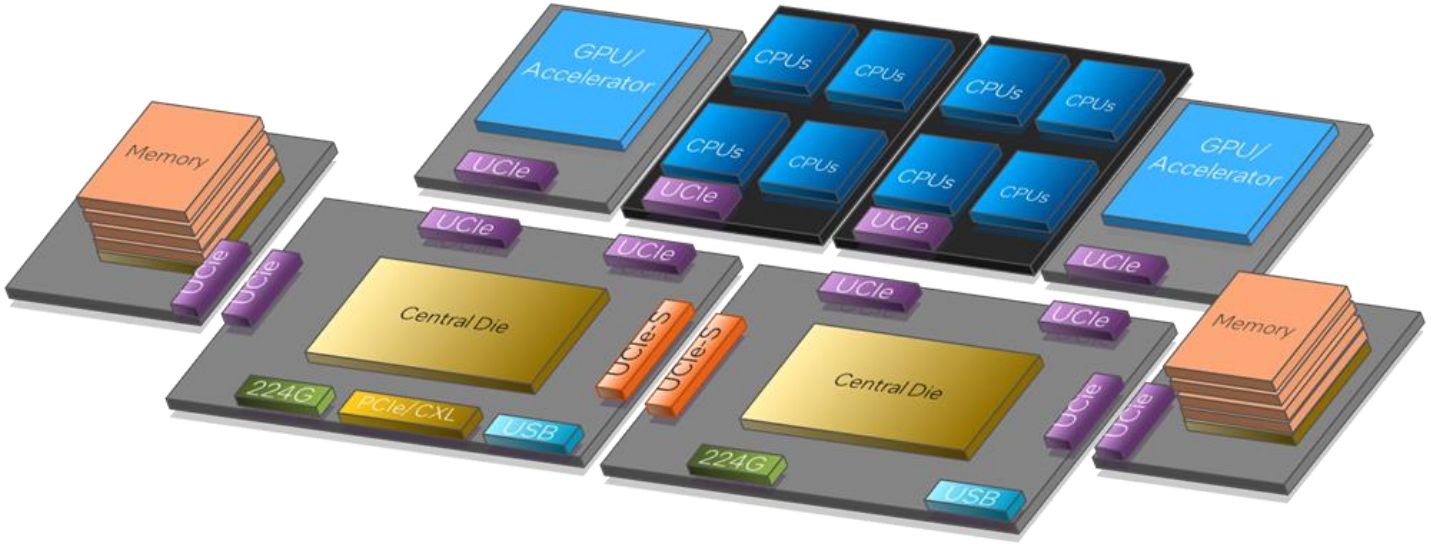
- Multiple chiplets from different vendors within a SiP:
  - Potentially using different technology nodes
  - Each with their own defined temperature reliability limits, beyond which transistor function is not guaranteed
  - Each with own temperature sensing capabilities and its known error bars; resulting in a defined max transistor Tj limit per chiplet
- SiPs are required to have mitigation mechanisms (reactive or proactive) to prevent hitting chiplet max Tj limits. Following mechanisms are required:
  1. **Fast throttle:** SIPs implement a fail-safe critical temp limit below the Tj max. Global fast throttle action is taken to keep the chiplet(s) below their critical limit(s).
  2. **Emergency Shutdown:** If the temp continues to rise and exceed Tjmax, SiP signals the power source to shutdown the supplies to prevent SiP/System damage or worse.

➢ **A standard approach across chiplet vendors is necessary to ensure critical function interoperability at the SiP level**

UCIe™ Universal Chiplet Interconnect Express

UCIe Usage Model: System in Package

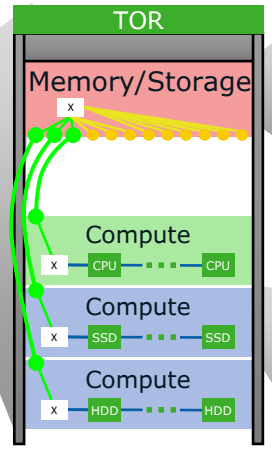
- SoC as a Package level construct
  - Standard and/ or Advanced package
  - Homogeneous/ heterogeneous chiplets
  - Chiplets from multiple suppliers
- Using planar (2D and 2.5D) and Vertical (3D) UCIe chiplets
- Across all segments:
  - Hand-held, Client, Server, Workstation, Automotive, Comms, HPC, etc.
  - Similar to PCIe/ CXL/ USB at board level



Off-Package Connectivity with UCIe Retimers: Composability at Rack/ Pod Level

Pod of Racks
Physical connectivity using UCIe-Retimer-based co-packaged optics carrying CXL protocol

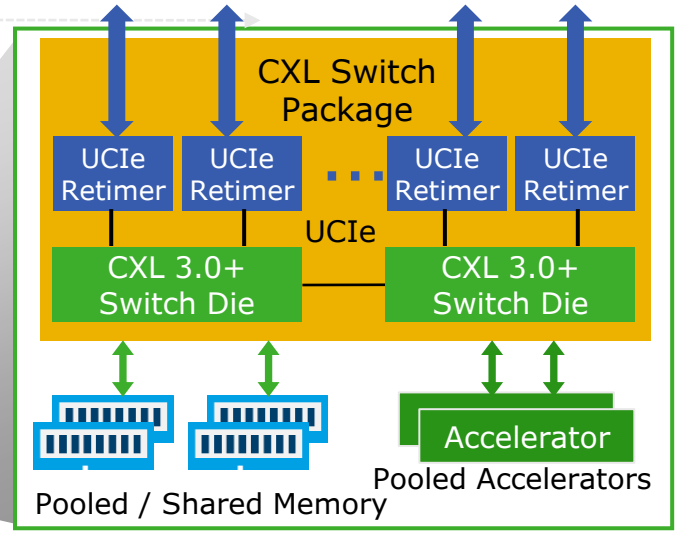
UCIe-based co-packaged Optics for Rack/Pod Level Connectivity running CXL protocol

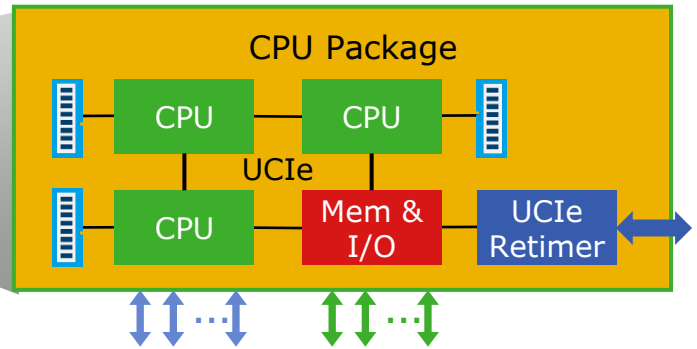


Pooled / Shared Memory Or Accelerator Drawer

Compute Drawer

Optical Connection for Intra-Rack and Pod





Optical Connection to CXL Switch on Rack

CXL/PCIe DDR

Interconnects at Drawer Level

UCIe™ Universal Chiplet Interconnect Express

Key Metrics with UCIe 3.0

Characteristics / KPIs	UCIe-S (2D)	UCIe-A (2.5D)	UCIe 3D	Comments
Characteristics				
Data Rate (GT/s)	4, 8, 12, 16, 24, 32, 48, 64		Up to 4	UCIe 3D SoC Logic frequency – power efficiency is critical Added 48G and 64G with UCIe 3.0
Width (each cluster)	16	64	80	UCIe 3D: Options or reduced width to 70, 60…
Bump Pitch (µm)	100 – 130	25 – 55	≤ 10 (optimized) > 10 – 25 (functional)	Must scale so that UCIe fits within the bump area, UCIe-3D must support hybrid bonding
Channel Reach (mm)	≤ 25	≤ 2	3D vertical	UCIe-3D: FtF, FtB, BtB, multi-stack possible
Target for Key Metrics				
BW Shoreline (GB/s/mm)	28 – 224 278, 370	165 – 1317 1975, 2634	N/A (vertical)	For UCIe-S and UCIe-A: First row is for 4-32G. Second Row is for 48G and 64G respectively. Numbers are for 45u (UCIe-A) and 110u (UCIe-S)
BW Density (GB/s/mm^2)	22 – 192	188 – 1646	4,000 (9µm) – 300,000 (1µm)	Numbers are for 45u (UCIe-A) and 110u (UCIe-S)
Power Efficiency Target (pJ/b)	0.5 (<=16 G) 0.75 (>= 32 G)	0.25 (<=12G) 0.3 (16G – 32G) 0.5 (>= 48G)	<0.05 at 9µm -> 0.01 at 1 µm	
Low-Power Entry/Exit	0.5nS ≤ 16G, 0.5-1nS ≥ 24G		0nS	No preamble or post-amble
Reliability (FIT)	0 < FIT (Failure in Time) << 1		0 < FIT << 1	
ESD	30V CDM		5V CDM → ≤ 3V	UCIe-3D: 5V CDM at introduction, no ESD for W2W hybrid bonding possible

UCIe continues to deliver compelling power-efficient and cost-effective performance

Future Directions and Conclusions

- UCIe Consortium is evolving UCIe technology in a backward-compatible manner comprehending new usage models supporting a plug-and-play open chiplet ecosystem
- UCIe is an open industry standard that establishes an open chiplet ecosystem and ubiquitous interconnect at the package level.
  - Tremendous support across the industry with several companies announcing products
  - UCIe 3.0 Specification is available to the public https://www.uciexpress.org/specification
- UCIe Consortium welcomes interested companies and institutions to join the organization at the Contributor or Adopter level.
- 6 Technical Working Groups (Electrical, Protocol, Form Factor/Compliance, Manageability/Security, Systems and Software, Automotive) alongside the Marketing Working Group are driving the technology toward the future.
  - Incredible innovations happening in the Consortium!
- The multi-decade journey is off to a great start!
- Get involved! Learn more by visiting www.UCIexpress.org

UCIe™ Universal Chiplet Interconnect Express

Questions?

Thank You

www.UCIexpress.org

UCIe™ Consortium 2025