UCIe Consortium Advances from Chiplet Connectivity to System-Level Integration with UCIe 4.0 Specification

Defines key features and requirements for chiplets to operate seamlessly as a system of chiplets.

Key highlights:

- **Enables scalable, high-performance on-package memory connectivity** with up to 93.75% data efficiency and approximately 2.5 TB/s/mm die-edge bandwidth density.
- **Improves power efficiency and bandwidth density** with a co-optimized link profile delivering up to 30-80% greater energy efficiency at 64 GT/s and an enhanced bump map providing approximately 20% greater shoreline and 10% greater area bandwidth density.
- **Expands UCIe from chiplet-level connectivity to secure, reliable system-level integration** through enhanced manageability, trusted chiplet reporting, protected management communications, reset management, error notification and link-health monitoring to ensure individual chiplets operate securely and reliably as part of a complete system.

Beaverton, Ore., U.S. – Nov. 12, 2026 – Today, the Universal Chiplet Interconnect Express® (UCIe®) Consortium, the open standards group for interconnects between chiplets within a package, announced the release of the UCIe 4.0 Specification, taking the UCIe architecture beyond chiplet-level interface design to address key requirements for integrating multiple chiplets into a cohesive on-package system.

As chiplet architecture grows more sophisticated, connectivity is only part of the challenge. Systems incorporating compute, accelerator, memory and other chiplets must also address how those components are managed, secured and monitored while efficiently using power, die area and package resources. The UCIe 4.0 Specification addresses these broader system-level requirements with new capabilities spanning manageability and security, efficiency, memory connectivity and reliability.

“UCIe is evolving from defining how individual chiplets connect to addressing what is required for multiple chiplets to function together as a system,” said Cheolmin Park, UCIe Consortium President and Samsung Corporate VP and Head of Package Marketing team at Samsung Electro-Mechanics. “With UCIe 4.0, we are extending the architecture with system-level manageability and security while continuing to improve memory connectivity, efficiency, and reliability. These capabilities provide a stronger foundation for building increasingly sophisticated heterogeneous systems around an open, interoperable chiplet ecosystem.”

Standardizing Memory and Increasing System Efficiency
The specification introduces a standardized on-package memory link between SoCs and memory logic chiplets, providing a power- and cost-efficient approach to scaling memory bandwidth using existing memory technologies. By leveraging the existing UCIe PHY and Adapter ecosystem, the UCIe.mem protocol simplifies memory integration while achieving data efficiency as high as 93.75% and die-edge bandwidth density of approximately 2.5 TB/s/mm. This combination delivers high throughput and enables memory bandwidth to scale with evolving system and workload requirements.

The newly released specification also gives designers new ways to improve system efficiency, including an optional power-optimized profile that delivers up to 30-80% greater energy efficiency at 64 GT/s and an enhanced bump map for UCIe-S 48 GT/s and 64 GT/s that increases bandwidth density while reducing the shoreline needed for high-speed die-to-die connectivity. The enhanced bump map provides approximately 20% greater shoreline bandwidth density and 10% greater area bandwidth density, letting designers achieve higher bandwidth in a given footprint or free package resources for other system needs.

Together, these enhancements give system designers additional flexibility to optimize bandwidth, power, area and memory resources across the package rather than treating each chiplet interface in isolation.

Advancing System-Level Security and Manageability
The UCIe 4.0 Specification introduces Trusted Reporting of Chiplet State (TRoCs) to support trusted reporting of chiplet state, helping the system establish confidence in information from individual chiplets, verify that they are operating as expected, and protect against spoofed or manipulated state information.

UCIe 4.0 introduces two-way integrity-protected management channels to help protect communication between chiplets from unauthorized modification and verify the integrity of management information. Together with enhanced reset management, these capabilities provide a more robust foundation for securely managing individual chiplets as part of a larger system.

UCIe 4.0 also introduces manageability and security capabilities for environments where multiple chiplets, potentially from different vendors and serving different functions, operate together within the same package.

Extending System-Level Reliability for Automotive Applications
The UCIe 4.0 Specification expands system-level capabilities with features supporting the growing adoption of chiplet architectures in automotive applications.

New optional error notifications and link-health monitoring provide greater visibility into interconnect integrity and potential failures, enabling systems to detect and respond to link issues. Standardized link-health information can also be incorporated into broader automotive reliability and functional-safety requirements, helping system designers monitor the health of chiplet interconnects as part of the overall vehicle system.

UCIe 4.0 Specification Highlights:

- **Standardized connectivity between SoCs and memory logic dies** simplifies memory integration, achieving up to 93.75% data efficiency and approximately 2.5 TB/s/mm die-edge bandwidth density for power- and cost-efficient scaling of on-package memory bandwidth as system and workload needs evolve.
- **Co-Optimized link profiles** deliver up to 30-80% greater energy efficiency, while the enhanced UCIe-S bump map for 48 GT/s and 64 GT/s provides ~20% greater shoreline and ~10% greater area bandwidth density to enable higher bandwidth, a smaller footprint, or more package resources for other system needs.
- **Enhanced security capabilities** introduce Trusted Reporting of Chiplet State (TRoCs) for trusted chiplet state reporting and integrity-protected management channels to secure communications from unauthorized modification.
- **System-level manageability** delivers enhanced reset management and greater chiplet-state visibility for reliable operation across integrated systems.
- **Optional error notifications and link-health monitors** provide greater visibility into interconnect integrity and potential failures for automotive reliability and functional-safety mechanisms.
- **Fully backward compatible with all previous UCIe specifications** for seamless integration and adoption.

The UCIe 4.0 Specification is available to the public by request at www.uciexpress.org/specifications.

Resources:

- UCIe 4.0 Specification
- UCIe 4.0 White Paper
- UCIe Consortium member statements of support

About the UCIe Consortium

The UCIe Consortium is an industry consortium dedicated to advancing UCIe® (Universal Chiplet Interconnect Express®) technology, an open industry standard that defines the interconnect between chiplets within a package, enabling an open chiplet ecosystem and ubiquitous interconnect at the package level. UCIe Consortium is led by key industry leaders Advanced Semiconductor Engineering, Inc. (ASE), Alibaba, AMD, Arm, Google Cloud, Intel Corporation, Meta, NVIDIA, Qualcomm Incorporated, Samsung Electronics, and Taiwan Semiconductor Manufacturing Company, and represents more than 150 member companies. For more information, visit www.UCIexpress.org.

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