UCIe® 4.0 Specification: Advancing Memory-Centric, Secure, and Reliable Heterogeneous Chiplet Systems

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Introduction

The semiconductor industry continues its transition toward open, heterogeneous chiplet-based architectures, driven by the need for greater performance, scalability, flexibility, cost-effectiveness, and faster innovation. As workloads such as artificial intelligence (AI), high-performance computing (HPC), cloud services, and data-centric applications grow in complexity, system designers are increasingly disaggregating functionality across multiple chiplets to optimize technology choices, improve time-to-market, and enable more efficient use of packaging resources. Universal Chiplet Interconnect Express® (UCIe®) has established itself as the open industry-standard interconnect for chiplet-based systems, providing a common framework that enables interoperable communication among heterogeneous chiplets from multiple suppliers and ecosystems. Building on the strong foundation established by previous generations, the UCIe 4.0 specification continues the evolution of the open chiplet ecosystem by expanding support for increasingly sophisticated chiplet-based systems and emerging memory-centric architectures.

The UCIe 4.0 specification introduces significant enhancements that improve memory scalability, bandwidth density, energy efficiency, security, manageability, and reliability while maintaining full backward compatibility with prior generations of UCIe. A key addition is **UCIe.mem**, a standardized architecture for memory connectivity that enables efficient, high-bandwidth, interoperable on-package memory expansion. Further innovations improve energy efficiency and bandwidth density through enhancements to the physical layer and package interface, enabling higher bandwidth delivery and more efficient utilization of package resources. UCIe 4.0 also introduces new security and trust capabilities, including trusted chiplet state reporting and integrity-protected management communications, along with enhanced system manageability features for operating increasingly complex multi-chiplet systems. New reliability and health-monitoring capabilities further support automotive and other mission-critical applications. Together, these advancements build upon prior generations of UCIe, delivering significant new capabilities for memory connectivity and expansion, enhanced bandwidth density and energy efficiency, security, system management, and reliability, all while maintaining the openness and interoperability that define the UCIe ecosystem. We encourage readers to review the white papers on UCIe 1.0, UCIe 1.1, UCIe 2.0, and UCIe 3.0 as well as our webinar recordings for additional background on the evolution of the UCIe architecture.

Standardized On-Package Memory Connectivity with UCIe.mem

The rapid growth of AI, HPC, cloud, and data-centric workloads continues to drive unprecedented demand for memory bandwidth and capacity. As compute performance scales through increasingly heterogeneous chiplet-based architectures, providing sufficient memory bandwidth has become one of the primary challenges in delivering balanced system performance. There is growing demand for a standardized approach that enables memory resources to be integrated and scaled across a broad ecosystem of interoperable chiplets and memory technologies.

To address these challenges, the UCIe 4.0 specification introduces UCIe.mem, a standardized architecture for memory connectivity that enables efficient, high-bandwidth, interoperable on-package memory expansion across a broad range of memory technologies. By leveraging the existing UCIe ecosystem, including the UCIe PHY, adapter, compliance framework, and packaging infrastructure, UCIe.mem provides a common foundation for connecting compute chiplets to memory resources while preserving the openness and interoperability that define the UCIe architecture.

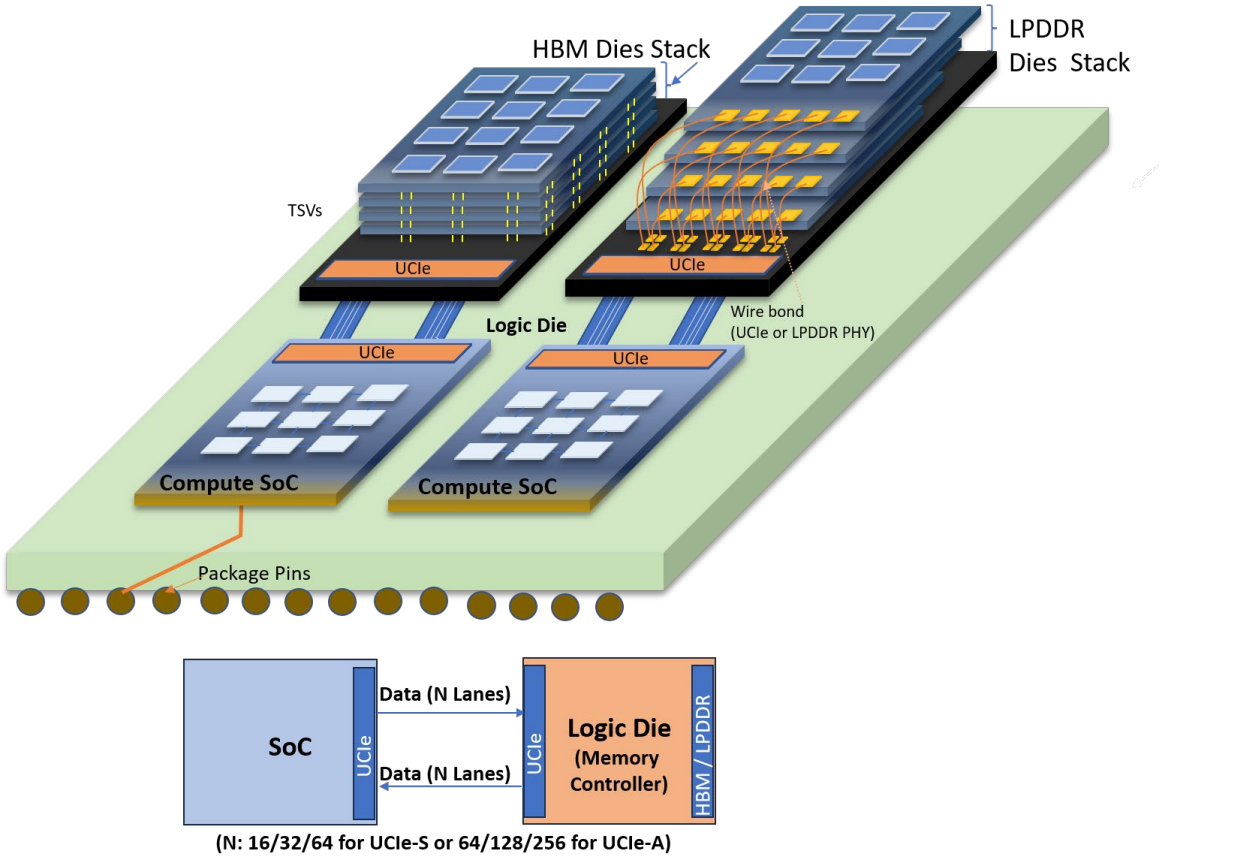


Figure 1: UCIe.mem architecture enabling standardized connectivity between compute SoCs and memory logic dies. Memory controllers within the logic die interface to HBM, LPDDR, or future memory technologies while communicating with compute chiplets through standard UCIe links.

As shown in Figure 1, UCIe.mem enables a compute SoC to communicate with a memory logic die through UCIe links (either UCIe-S or UCIe-A). The logic die contains the memory controller and interfaces to one or more memory technologies such as HBM or LPDDR. This architecture enables memory subsystem disaggregation while preserving a standardized interface between compute and memory resources. By separating memory control functions from the compute device while using a

standardized die-to-die interconnect, UCIe.mem provides a scalable architecture for expanding memory bandwidth and capacity across heterogeneous chiplet-based systems.

UCIe.mem utilizes native split-transaction, memory-semantic protocols optimized for efficient operation across symmetric UCIe links. Rather than transporting low-level DRAM interfaces across chiplet boundaries, memory accesses are abstracted into requests and responses that are efficiently carried over the UCIe fabric. To maximize effective bandwidth, UCIe.mem defines optimized protocol encodings that efficiently pack memory requests and responses within UCIe flits while minimizing protocol overhead. For example, UCIe.mem defines optimized encodings that enable two memory requests or four memory responses to be packed within the 16-byte slots of a 256-byte flit. This approach significantly reduces the impact of headers, acknowledgments, reliability mechanisms, and flow-control information. As a result, read-intensive traffic can achieve approximately 94% data efficiency across 64-byte, 128-byte, and 256-byte payloads, enabling more of the available link bandwidth to be devoted to application data transfer.

By standardizing memory connectivity at the chiplet level, UCIe.mem provides a scalable and interoperable foundation for current and future memory technologies, enabling memory-centric heterogeneous chiplet systems that can evolve alongside future packaging, memory, and compute innovations.

Enhanced Bandwidth Density and Energy Efficiency

As AI, HPC, and other bandwidth-intensive applications continue to scale, die-edge shoreline and power consumption are increasingly becoming limiting factors in system design. UCIe 4.0 introduces two complementary sets of enhancements that improve bandwidth delivery and energy efficiency while maintaining interoperability and backward compatibility with existing UCIe implementations. The resulting key performance indicators are summarized in Table 1.

The first enhancement improves shoreline bandwidth density for UCIe-S operating at 48 GT/s and 64 GT/s. To address die-edge constraints in bandwidth-hungry applications such as AI and HPC, UCIe 4.0 introduces an enhanced bump map that reduces shoreline requirements by approximately 20%, increasing shoreline bandwidth density by approximately 20% while increasing areal bandwidth density by approximately 10%. The enhanced bump map standardizes on a common 1143 µm shoreline dimension across high-speed UCIe-S implementations, providing greater packaging flexibility while simplifying integration.

The second enhancement introduces co-optimized link profiles that can reduce link power consumption by 30-80% in environments where the characteristics of the partner chiplet are known and specific design assumptions can be made. These profiles are applicable to both UCIe-S and UCIe-A and are intended for implementations where the communicating chiplets use compatible process technologies, can share common voltage rails, and, in the case of UCIe-S, operate across optimized short-reach channels. To achieve these gains, UCIe 4.0 incorporates several architectural and circuit-level optimizations, including UCIe-3D style transmit-receive clocking, QDR signaling, direct sampling, optimized equalization, adaptive voltage and termination control, low-swing signaling, and enhanced timing-tracking mechanisms. These profiles maintain compatibility with the corresponding UCIe-S and UCIe-A bump maps while providing substantial energy-efficiency improvements. Additional optional optimizations, including asymmetric-width configurations, further enhance implementation flexibility.

Characteristics / KPIs	UCIe-S (2D)	UCIe-A (2.5D)	UCIe 3D
Characteristics			
Data Rate (GT/s)	4, 8, 12, 16, 24, 32, 48, 64		Up to 4
Width (each cluster)	16	64	80
Bump Pitch (µm)	100 – 130	25 – 55	≤10 (optimized) > 10 – 25 (functional)
Channel Reach (mm)	≤ 25	≤ 2	~0 (in µm)
Target for Key Metrics			
BW Shoreline (GB/s/mm @ bump pitch listed)	28 (4G) – 448 (64G) (@ 110 µm)	165 (4G) – 2634 (64G) (@ 45 µm)	N/A (vertical)
BW Density (GB/s/mm^2, @ bump pitch listed)	22 (4G) – 214 (64G) (@ 110 µm)	188 (4G) – 1646 (64G) (@ 45 µm)	4,000 (@ 9µm 4G) - 300,000 (@ 1µm 4G)
Energy Efficiency (pJ/b) (at 0.5V)	0.5 (≤ 16G) 0.75 (>16G)	0.25 (≤12G) 0.3 (16-32G) 0.5 (≥48G)	< 0.05 at 9µm – < 0.02 at 3µm
	0.1(<=8G), 0.15 (12G, 16G), 0.2 (24G, 32G), 0.3 (>=48G) [with co-optimization]		
Low-Power Entry/Exit	0.5ns ≤16G, 0.5-1ns ≥24G		0ns
Reliability (FIT)	0 < FIT (Failure in Time) << 1 BER: 10^{-12}, 10^{-15}, 10^{-27} (data rate dependent)		0 < FIT << 1 BER: 10^{-27}
ESD	30V CDM		5-V CDM –> ≤ 3 V

Table 1: Key performance indicators of UCIe 4.0, including shoreline bandwidth density improvements and the energy-efficiency gains enabled by co-optimized UCIe link profiles

Secure and Trusted Chiplet Systems

As heterogeneous chiplet systems continue to evolve, packages incorporate compute, memory, I/O, and accelerator chiplets from multiple suppliers, each with its own lifecycle management, security capabilities, and test interfaces. Establishing trust across these independently developed components is a critical system-level requirement. System firmware and management software must be able to verify the identity, security status, and operational state of participating chiplets and establish confidence in the information they report. UCIe 4.0 introduces new capabilities that strengthen security and trust across multi-vendor chiplet systems while preserving the openness and interoperability of the UCIe ecosystem.

Trusted Reporting of Chiplet State (TRoCs): UCIe 4.0 introduces the Trusted Reporting of Chiplet State (TRoCs) capability, a standardized framework for trusted reporting of chiplet lifecycle state, security status, and test-interface configuration through the existing register-based UCIe Memory Access Protocol. As illustrated in Figure 2, TRoCs capabilities are distributed across participating chiplets, enabling a primary system Root of Trust (RoT) to establish trust throughout a heterogeneous package consisting of compute, memory, I/O, and accelerator chiplets.

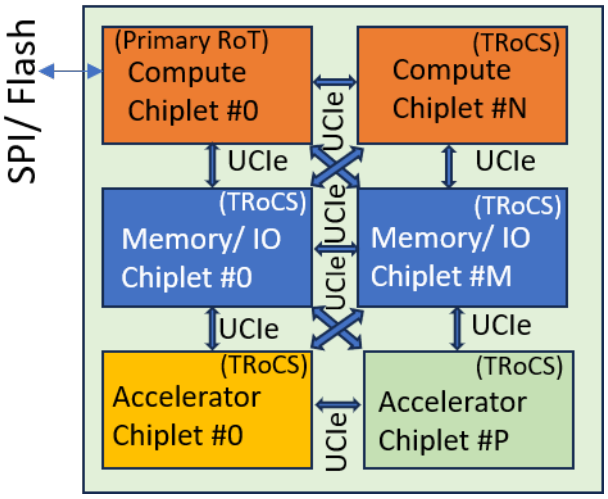


Figure 2: Trusted Reporting of Chiplet State (TRoCs) enables a primary Root of Trust (RoT), also referred to as the Security Director, to establish trust across chiplets through standardized reporting of chiplet identity, lifecycle state, and security status.

TRoCs enables a primary Root of Trust to securely query and validate the state of participating chiplets through cryptographically protected challenge-response mechanisms. By establishing confidence in reported lifecycle, security, and test-interface status, TRoCs helps protect against spoofing, replay, and man-in-the-middle attacks while enabling secure operation across independently developed chiplets from multiple vendors.

Two-Way Integrity-Protected Management Communications: Building on the trusted chiplet-state reporting provided by TRoCs, UCIe 4.0 extends protection to management communications exchanged across the heterogeneous SiP illustrated in Figure 2. Because management packets may traverse intermediate chiplets or interposer infrastructure, endpoints need to verify that commands originated from an authorized Root of Trust (RoT), also referred to as the Security Director, and were not modified or replayed in transit. This protection helps prevent the spoofing of security-clearance information or unauthorized changes to sensitive test and debug capabilities.

UCIe 4.0 provides two-way cryptographic integrity protection for management channels over the existing Management Transport Protocol. A secure session is established between the Security Director and each management endpoint and renewed following a SiP or chiplet reset. The key-establishment approach, based on NIST SP 800-56C, supports endpoints with or without their own entropy source or random-number generator. Multiple session keys may be derived to provide integrity protection and, where required, confidentiality; the Security Director may also provision keys for protected communication between management endpoints. Together with TRoCs, this capability provides trusted state reporting and integrity-protected management communications across heterogeneous multi-vendor chiplet systems.

Enhanced System Manageability

As heterogeneous chiplet systems continue to grow in complexity, system integration and operational management are becoming increasingly important. UCIe 4.0 introduces several enhancements that simplify provisioning, configuration, monitoring, and lifecycle management across multi-vendor chiplet systems.

Asset Provisioning: As heterogeneous chiplet systems incorporate components from multiple vendors, assets required for system integration may need to be provisioned after chiplet manufacturing and during system operation. These assets can include identifiers, configuration information, and security credentials. UCIe 4.0 introduces a standardized framework for asset provisioning, built upon the existing UCIe Memory Access Protocol, to provide a common mechanism for provisioning assets across chiplets from different suppliers. By eliminating vendor-specific provisioning methods, this approach simplifies SiP integration, reduces deployment complexity, and enables scalable, interoperable multi-vendor chiplet systems.

Chiplet-Level Reset Management: Chiplets commonly implement Power-on, Cold, and Warm Reset, but their behavior, interfaces, and control mechanisms may differ across vendors. In addition to the existing UCIe Domain Reset for the die-to-die interface, UCIe 4.0 standardizes consistent behavior for Power-on, Cold, and Warm Reset across independently developed chiplets. Power-on Reset is de-asserted after the power rails are stable. Cold Reset returns the chiplet to its power-on default state, while Warm Reset supports controlled recovery by allowing selected vendor-defined state to be preserved. The specification also defines mandatory Cold and Warm Reset inputs, associated electrical and timing requirements, and a register-based Reset Capability for initiating resets and reporting reset status and cause. SiP-level reset causes, topology, and orchestration remain implementation-specific

Management Events: As heterogeneous SiPs become increasingly sophisticated, relying on software to poll individual chiplets for changes in status can increase management traffic and delay system response. UCIe 4.0 introduces an optional, event-driven framework that enables Management Elements to notify event targets as required. The framework supports discovery, configuration, delivery, optional acknowledgment and logging, and rate limiting mechanisms to prevent event storms from overwhelming the management network.

Two complementary delivery mechanisms address different performance requirements while providing implementation flexibility to support a broad range of events, triggering conditions, and system responses within the standardized framework. *Message-based events* use the existing Management Transport Protocol and UCIe Memory Access Protocol, with a delivery target below 1 µs between adjacent chiplets over a single sideband hop. *Priority Sideband Events (PSEs)* provide a more direct path for latency-critical notifications, targeting delivery below 100 ns between physically adjacent chiplets and supporting routing across multiple chiplets.

Reliability and Functional-Safety Support

Automotive and other mission-critical systems require robust runtime mechanisms for detecting, reporting, and responding to failures, including conditions in which normal communication paths may be unavailable. UCIe already provides continuous CRC protection, runtime parity-flit injection for lane-level error detection, and standardized eye-margin reporting following link training. UCIe 4.0 builds upon these capabilities with independent failure notification and additional visibility into link health. These features can be incorporated into broader system-level reliability and functional-safety architectures while allowing implementations to select the mechanisms appropriate to their use cases.

Independent Fail Indication: UCIe 4.0 introduces a dedicated, one-way open-drain signal for reporting critical failures originating within the UCIe interface or the broader chiplet. Independent of the UCIe mainband and sideband interfaces, and optionally powered from an isolated domain, the

signal supports failure notification when normal communication is unavailable while reducing exposure to common-cause failures.

Mission-Mode Link-Health Monitoring: For applications requiring additional runtime diagnostics, UCIe 4.0 enables optional eye-margin measurements without interrupting normal link operation. The resulting margin information can be incorporated into broader system-level monitoring and functional-safety mechanisms.

Conclusions

The UCIe 4.0 specification represents a significant advancement in open chiplet interconnect technology, addressing the increasingly demanding requirements of sophisticated heterogeneous systems. With standardized on-package memory connectivity, improved bandwidth density and energy efficiency, enhanced security and manageability, and expanded reliability and functional-safety support, UCIe 4.0 enables more scalable, efficient, secure, and robust chiplet-based systems. These advancements build upon prior generations while maintaining full backward compatibility and the openness and interoperability that define the UCIe ecosystem. As computing architecture continues to evolve, UCIe 4.0 provides a strong foundation for memory-centric heterogeneous systems across the compute continuum.