Driving the Future of Automotive Compute with UCIe

Automotive Working Group (AWG) Webinar

Meet the Presenters

Bala Chavali

Fellow @ AMD

UCIe Consortium AWG Co-Chair

Dr. Ericles Sousa

Sr. Principal Design Eng. @ Cadence

FuSa and Cybersecurity Certified Professional

UCIe Consortium AWG Co-Chair

Agenda

- Introducing UCIe
- Overview of UCIe 1.0 and after
- Automotive Use Case, Requirements, and Features
  - What is Automotive Working Group (AWG) Addressing
  - Adapter Layer Reliability Features
  - Physical Layer Reliability Features
  - Availability Features Mapped to UCIe
  - UCIe Capabilities Relevant to Functional Safety
- UCIe 3.0 Enhancements Relevant to Automotive
- Future Direction and Conclusions

Universal Chiplet Interconnect Express™ (UCIe™)
An Open Standard for Chiplet Development

- UCIe Guiding Principles
  - Open chiplet ecosystem
  - Backward-compatible evolution to ensure investment protection
  - Optimized power, performance, and cost metrics applicable across the entire compute continuum
  - Continuously innovate to meet the needs of the evolving ecosystem

Leveraging decades of experience driving successful industry standards at the board level: PCIe, CXL, USB, etc.

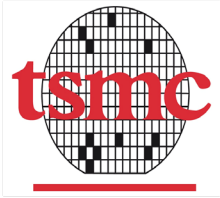
High-bandwidth, Low-latency, Power-efficient, Cost-effective Interconnects for
AI, HPC, Cloud, Edge, Enterprise, 5G, Automotive, Handhelds

UCIe Universal Chiplet Interconnect Express

Board Members

Leaders in semiconductors, packaging, IP suppliers, foundries, and cloud service providers are joining together to drive the open chiplet ecosystem.

JOIN US!



140+ Member Companies…and growing!

UCIe Universal Chiplet Interconnect Express

UCIe Consortium is Open for Membership

- UCIe Consortium welcomes interested companies and institutions to join the organization at the **Contributor and Adopter level**.

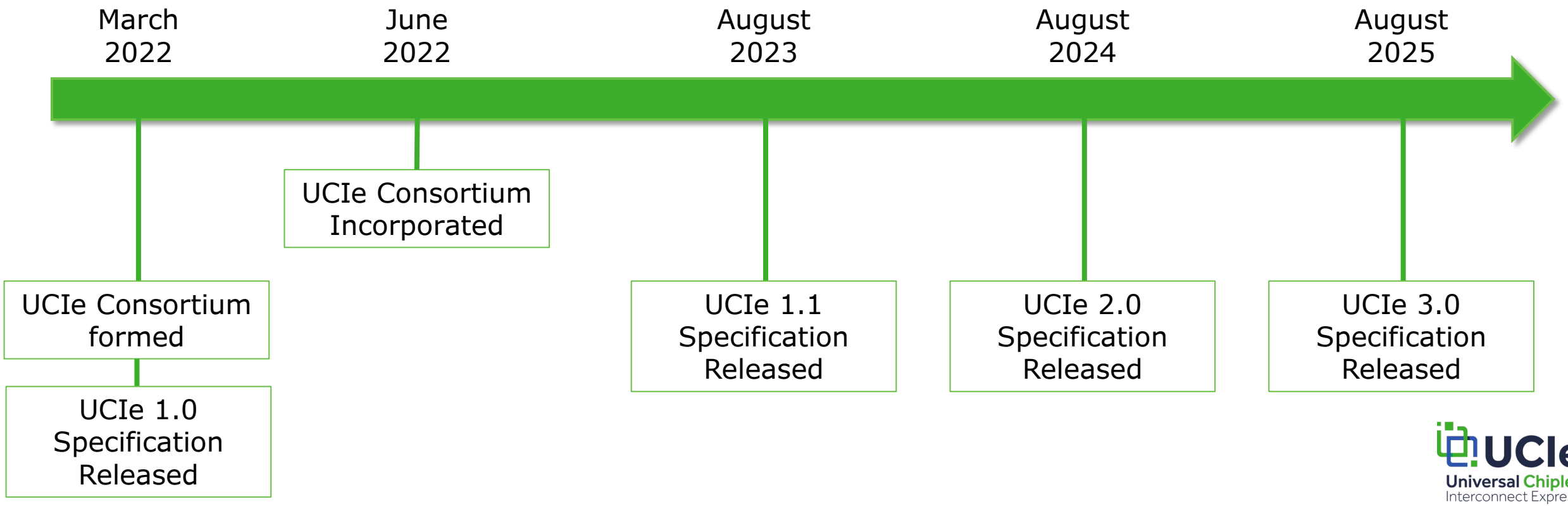
- UCIe was founded in March 2022 and incorporated in June 2022. Two levels of membership: Contributor and Adopter

- **Contributor Membership**
  - Access the Final Specifications (ex: 1.0, 1.1, 2.0, etc.)
  - Implement with the IP protections as outlined in the Agreements
  - Right to attend Corporation trade shows or other industry events as determined by the Board
  - Participate in the technical working groups
  - Influence the direction of the technology
  - Access the intermediate (dot level) specifications
  - Election to get to the Promoter Class/Board every year when the term of half the board members completes

- **Adopter Membership**
  - Access the Final Specifications (ex: 1.0, 1.1, 2.0, etc.), but not intermediate level specifications
  - Implement with the IP protections as outlined in the Agreements
  - Right to attend Corporation trade shows or other industry events as determined by the Board

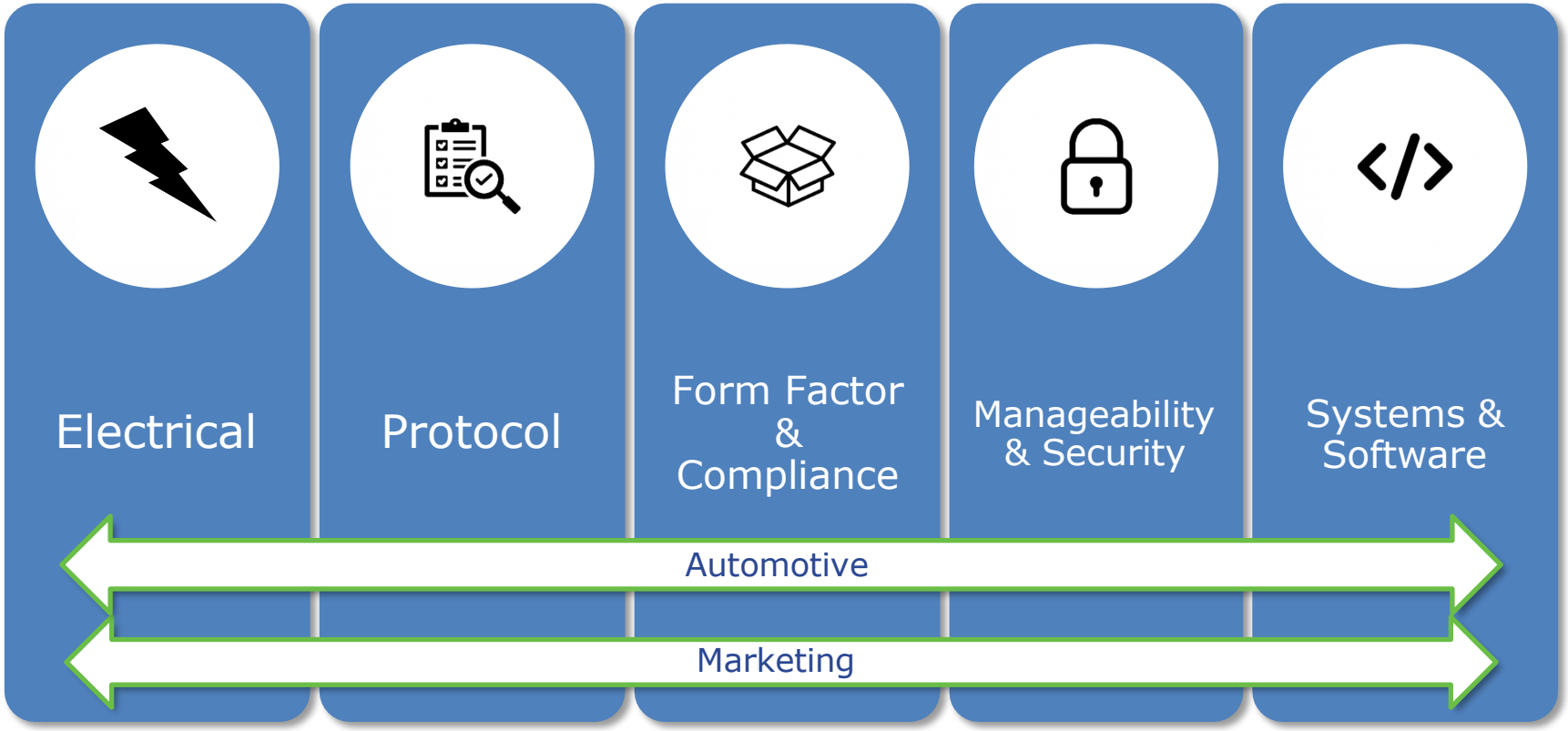
UCIe Universal Chiplet Interconnect Express

Member-Driven Evolution



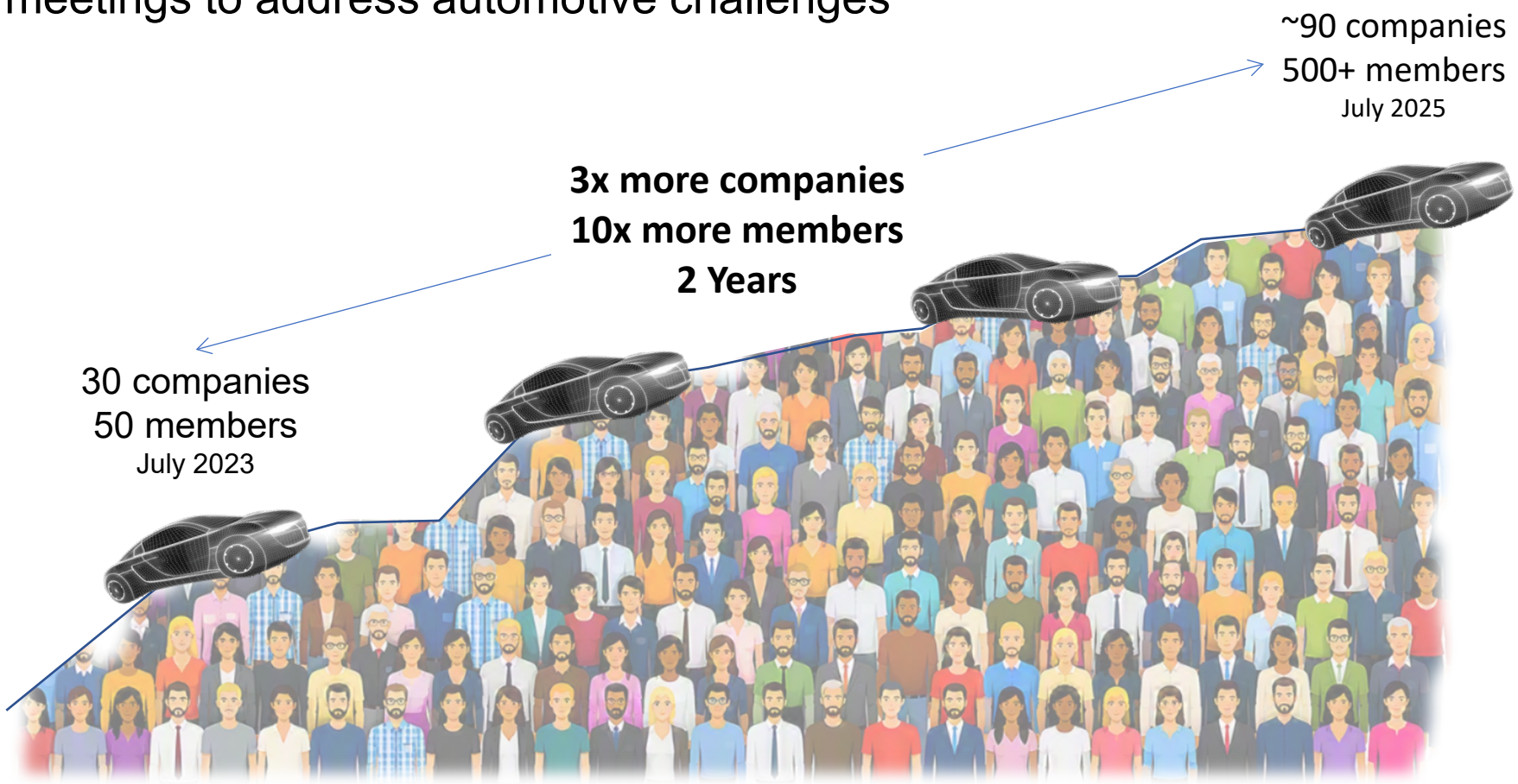
UCIe Consortium Working Groups

Working Groups are identifying and addressing the demands of a complete, full-stack solution for strengthening the open standards-based ecosystem.

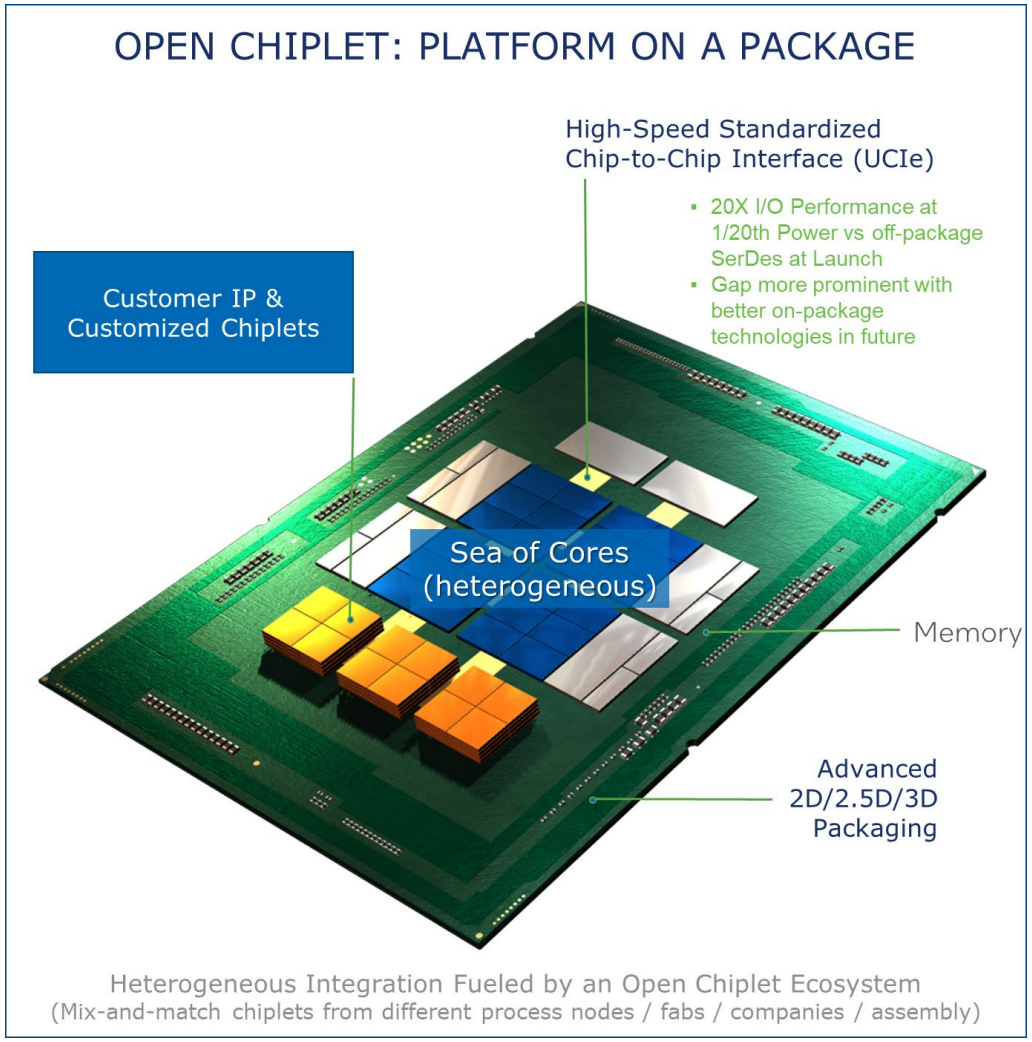


UCIe AWG in Numbers

- We cover the automotive chiplet market, including reliability, functional safety, and quality
- Biweekly meetings to address automotive challenges



Motivation for UCIe



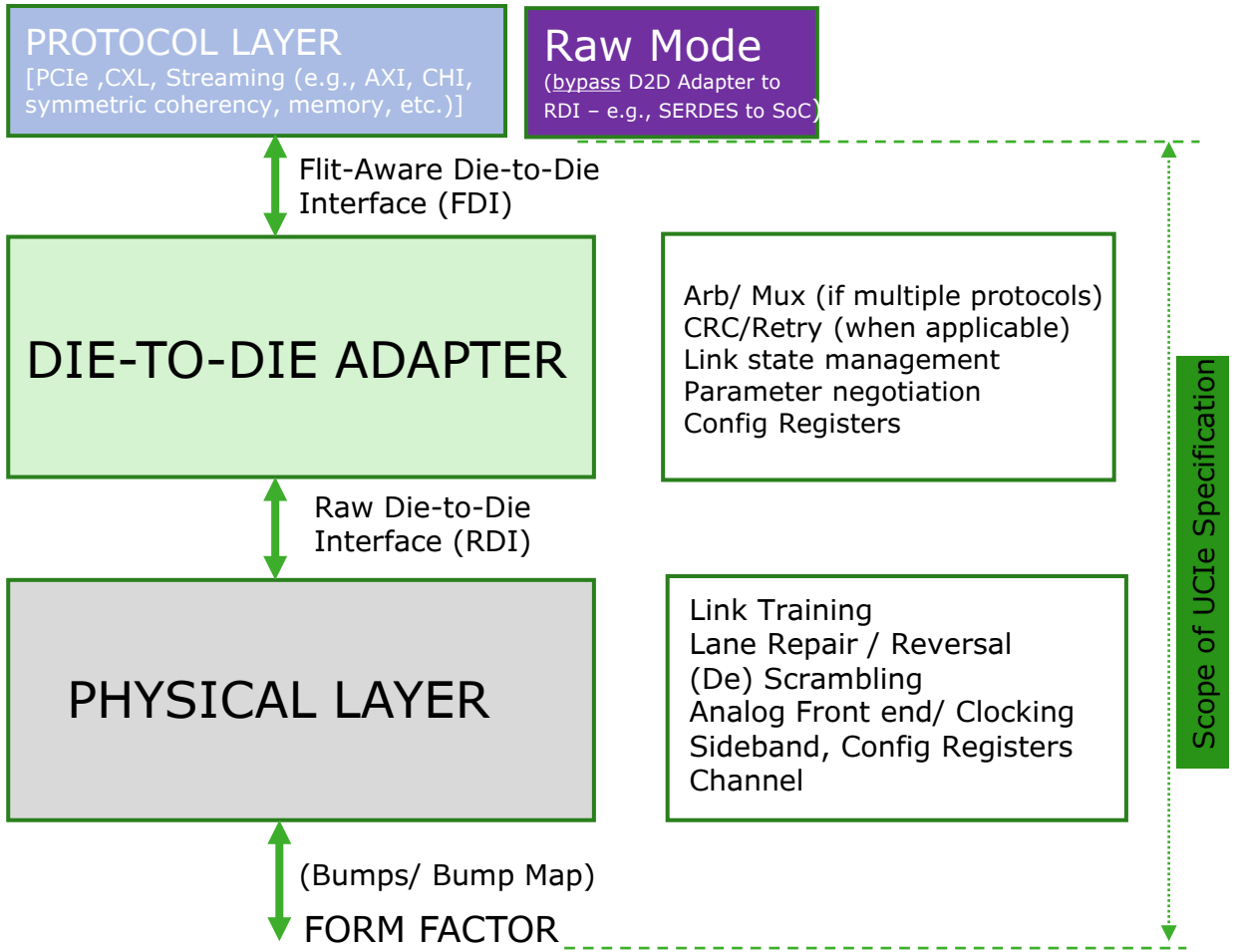
- Overcome reticle limits – SoC is now at package level
- Reduces time-to-solution (e.g., enables die reuse)
- Lowers portfolio cost (product & project)
  - Optimal process
  - Smaller dies => better yield
  - Reduces IP porting costs
  - Lowers product SKU cost
- Bespoke solution
  - Mix-and-match with a standard interface
- Scales innovation (Mfg. process locked IPs)

UCIe driving Industry alignment! Package is the new platform!

UCIe Universal Chiplet Interconnect Express

UCIe 1.0 and 1.1 Specifications for Planar Interconnects

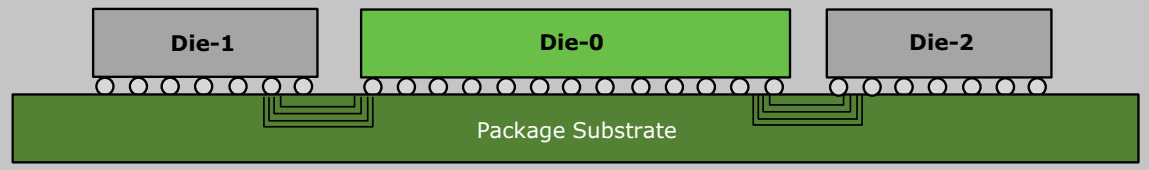
- **Layered Approach - industry-leading KPIs**
- **Planar: UCIe-S (2D) and UCIe-A (2.5D)**
- **Physical Layer:** Die-to-Die I/O
- **Die to Die Adapter:**
  - Reliable delivery, Multi-protocol support
- **Protocol**:
  - Usages: I/O attach, Memory, Accelerator
  - **Streaming for other protocols**
    - Scale-up (e.g., CPU/ GP-GPU/Switch from smaller dies)
- **Well-defined specification**
  - Configuration register for discovery and run-time
  - Form-factor and Management
  - Compliance for interoperability
  - Plug-and-play IPs with RDI/ FDI interface



More Information at: www.uciexpress.org (whitepapers and webinars):
-White Paper: https://www.uciexpress.org/ucie-resources: "UCIe: Building an open chiplet ecosystem"
-Webinars: https://www.uciexpress.org/webinars: "Introduction to UCIe" (Feb 21, 2023) and "UCIe 1.1 Specification" (Oct 12, 2023).

UCIe Universal Chiplet Interconnect Express

UCIe 1.0/1.1: Supports Standard and Advanced Packages

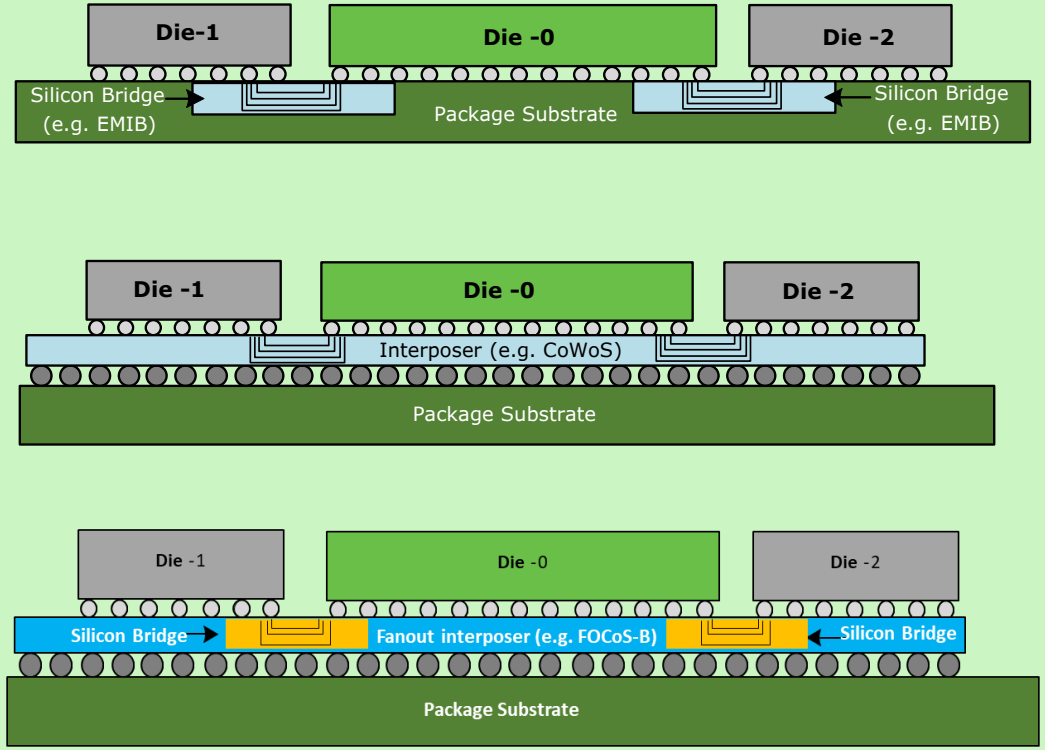


(Standard Package)

Standard Package: 2D – cost-effective, longer distance

Advanced Package: 2.5D – power-efficient, high bandwidth density

Dies can be manufactured anywhere and assembled anywhere – can mix 2D and 2.5D in same package: Flexibility for SoC designer

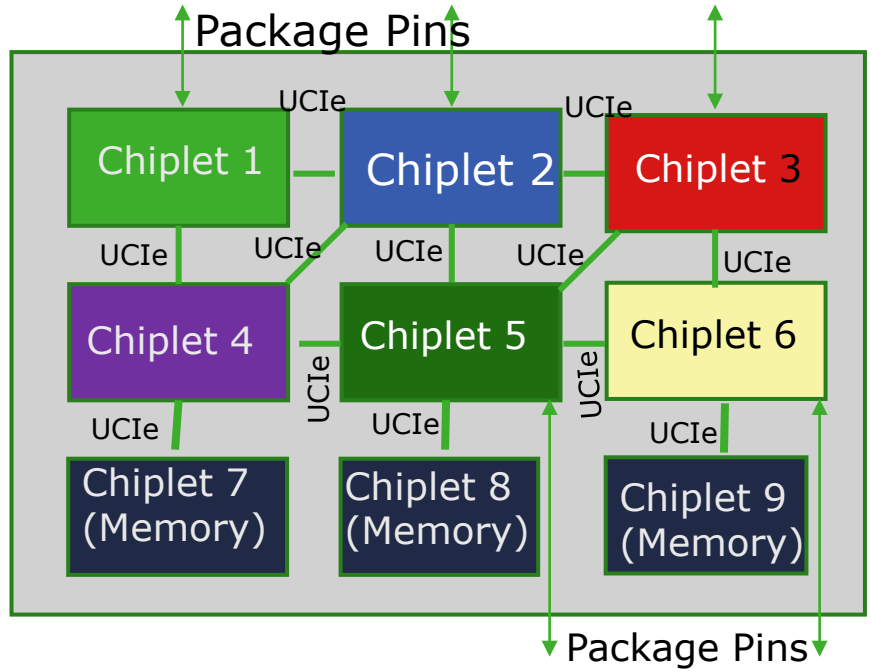


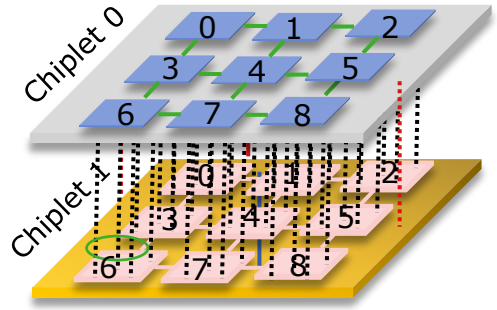
(Multiple Advanced Package Options)

More Information at: https://www.uciexpress.org/webinars : "UCIe Packaging Technologies" (June 15, 2023) and "Exploring the Advancement of Chiplet Technology and the Ecosystem" (April 17, 2024)

UCIe 2.0: Testability, Manageability, Debug, Vertical Chiplets with UCIe-3D

- Test: Die/Sort, Package/Bond
  - Micro-bumps can not be probed
  - Use other bumps (e.g., JTAG, UCIe-S)
- Repair: assembly & in field (UCIe)
- Debug and Manageability with security
  - lab, field – no analyzer/scope
- Some chiplets may not have access to package pins
  - Use UCIe-S (dedicated or shared, sideband only or mainband) to access remote chiplets from chiplets with package pins
- Definition of management fabric comprising of ports, elements, a director communicating through packets and software infrastructure leveraging industry standards like MCTP, supporting a wide range of bandwidth demands
- UCIe-3D delivers power-efficient performance comparable/ better than a large monolithic die



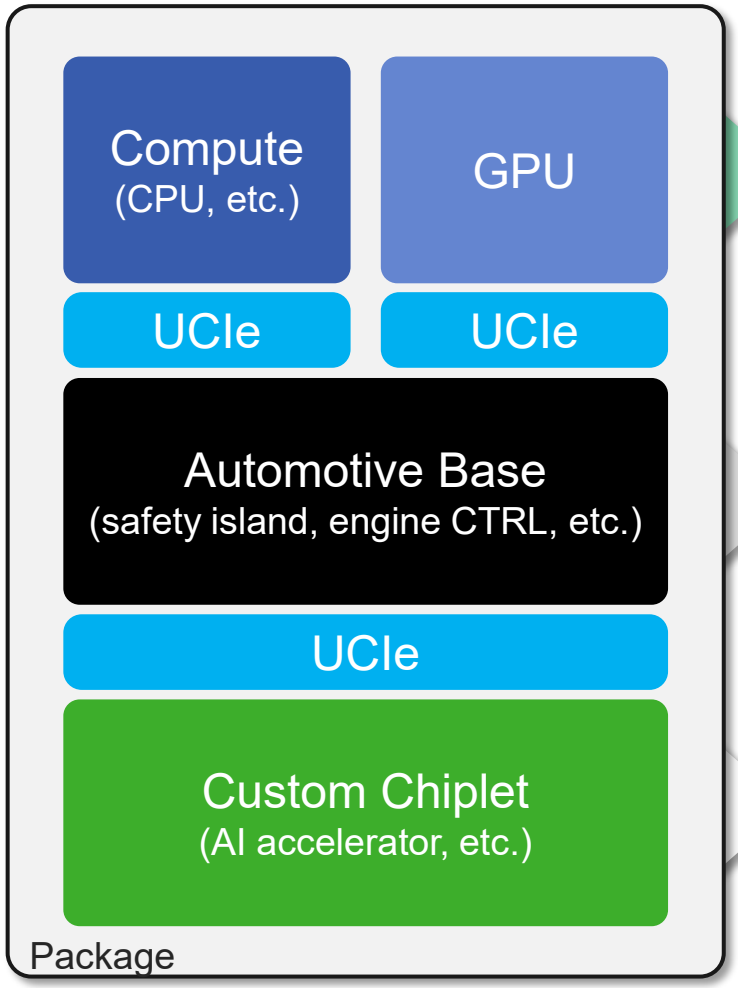


A common UCIe test/debug/management infrastructure that can work through the entire lifecycle with UCIe 2.0

Agenda

- Introducing UCIe
- Overview of UCIe 1.0 and after
- Automotive Use Case, Requirements, and Features
  - What is Automotive Working Group (AWG) Addressing
  - Adapter Layer Reliability Features
  - Physical Layer Reliability Features
  - Availability Features Mapped to UCIe
  - UCIe Capabilities Relevant to Functional Safety
- UCIe 3.0 Enhancements Relevant to Automotive
- Future Direction and Conclusions

Automotive UCIe Use cases



An Example of a Generic Chiplet-Based SoC

- Scalability and short innovation cycles
- Chiplets reuse ensuring functional scalability

- Compliant with the highest functional safety requirements
- Freedom from Interference
- Reliable for automotive use-cases

- Differentiation
- Demand for customization
- Inclusion of dedicated custom chiplets

UCIe
Universal Chiplet Interconnect Express

What is Automotive Working Group (AWG) Addressing

- Interoperability
  - Multi-vendor chiplets
- Reliability
  - Robust operation across long lifecycles
- Diagnostics
  - System-level visibility into link health
- Functional Safety Integration
  - UCIe capabilities are mapped to Functional Safety Architectures and Standards (Ex: ISO 26262)
- Qualification
  - Automotive deployment expectations
- *The AWG does not redefine the UCIe specification. It helps identify automotive requirements and promote ecosystem alignment.*

Adapter Layer Reliability Features

- The Adapter Layer provides several reliability-related functions:
  - CRC generation and checking
  - Retry support
  - Parity protection modes
  - Link-state management

Physical Layer Reliability Features

- The Physical Layer includes:
  - Link initialization
  - Link training
  - Sideband management
  - Lane management
  - Lane repair
  - Calibration and recalibration

Availability Features Mapped to UCIe

- UCIe defines spare lanes and repair capabilities that allow operation to continue even when certain lane defects are detected.
- Focus areas:
  - Fault handling
  - Link resiliency
  - Availability

UCIe Capabilities Relevant to Functional Safety

- UCIe specification provides communication robustness features such as:
  - CRC-based error detection
  - Retry mechanisms
  - Parity protection
  - Link-state monitoring
  - Lane repair
  - Error reporting
  - Management interfaces

Agenda

- Introducing UCIe
- Overview of UCIe 1.0 and after
- Automotive Use Case, Requirements, and Features
  - What is Automotive Working Group (AWG) Addressing
  - Adapter Layer Reliability Features
  - Physical Layer Reliability Features
  - Availability Features Mapped to UCIe
  - UCIe Capabilities Relevant to Functional Safety
- UCIe 3.0 Enhancements Relevant to Automotive
- Future Direction and Conclusions

UCIe 3.0 Enhancements Relevant to Automotive

- Enhanced recalibration mechanisms
  - Allows the transmitter (not just the receiver) to adjust clock-to-data skew during runtime recalibration of an active link

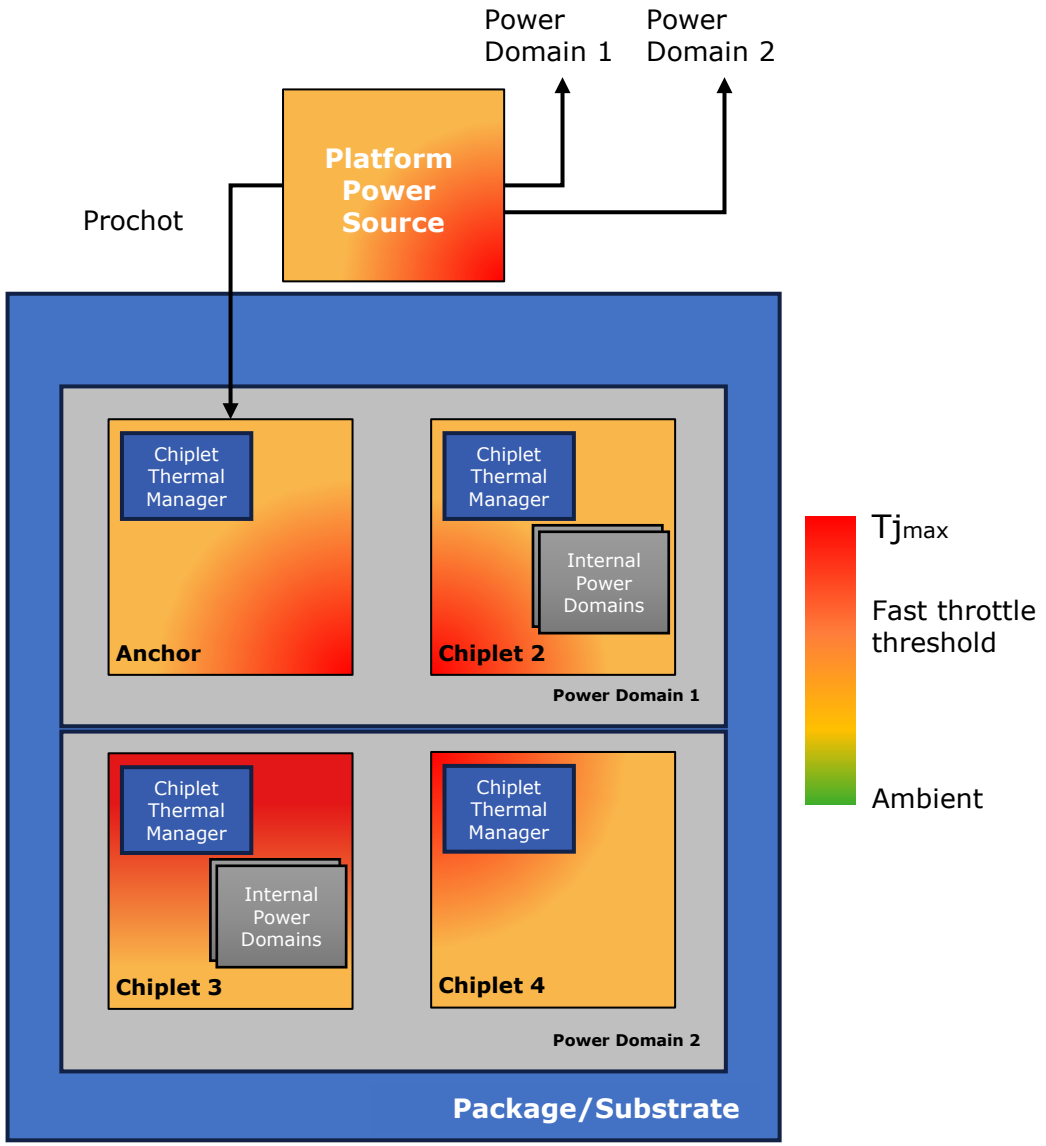
- Enhanced management capabilities
  - Shutdown and fast throttle
  - Extended-reach sideband support
  - Priority sideband packets

- *These improvements support higher-performance and more robust integration platforms.*

UCIe 3.0 Detail: Sideband Robustness for System-in-Package

- Extended-Reach Sideband (UCIe-S)
  - Extends the sideband-only reach from the UCIe 2.0 specification of 25 mm to 100 mm at 800 MHz operation
  - Enables a practical star topology in System-in-Package designs, connecting a Director chiplet directly to each chiplet for better manageability and security
  - Guidelines defined for signal levels and driver output resistance to preserve eye height/width margin over the longer channel
- Priority Sideband Packets
  - Motivation: some events — power down, power wake-up, low-latency telemetry, redundant power-supply switchover — need 1–10 µs notification and cannot be stuck behind routine traffic such as firmware downloads or debug dumps
  - Mechanism interrupts normal sideband traffic to insert a priority vector, with a bounded worst-case transfer time of 48 UI (about 60 ns)
- Improves diagnosability and deterministic response time for safety- and power-critical events in a multi-chiplet automotive SiP.

Fast Throttle and Emergency Shutdown



Problem Statement/Motivation

- Multiple chiplets from different vendors within a SiP:
  - Potentially using different technology nodes
  - Each with their own defined temperature reliability limits, beyond which the transistor function is not guaranteed
  - Each with its own temperature sensing capabilities and its known error bars, resulting in a defined max transistor Tj limit per chiplet
- SiPs are required to have mitigation mechanisms (reactive or proactive) to prevent hitting chiplet max Tj limits. The following mechanisms are required:
  1. **Fast throttle:** SIPs implement a fail-safe critical temp limit below the Tj max. Global fast throttle action is taken to keep the chiplet(s) below their critical limit(s).
  2. **Emergency Shutdown:** If the temp continues to rise and exceed Tjmax, SiP signals the power source to shut down the supplies to prevent SiP/System damage or worse.

➢ **A standard approach across chiplet vendors is necessary to ensure critical function interoperability at the SiP level**

Future Direction and Conclusions

- UCIe provides a standardized, open interconnect foundation with reliability, diagnostics, and management capabilities relevant to automotive systems
- The Automotive Working Group is aligning ecosystem requirements - interoperability, reliability, diagnostics, functional safety integration, and qualification - with UCIe's spec-defined capabilities
- UCIe 3.0 enhancements further strengthen automotive-relevant robustness
  - 48/64 GT/s, enhanced recalibration, extended-reach sideband, and more
- Get involved!
  - Learn more at www.UCIexpress.org

UCIe Universal Chiplet Interconnect Express

Questions?

Thank You

www.UCIexpress.org